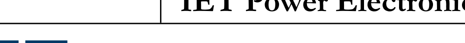

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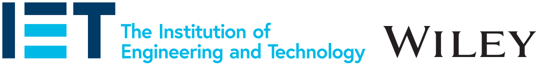

ORIGINAL RESEARCH

Design and validation of a novel semiconductor area optimised 3300 V SiC half bridge for MMC

Lukas Bergmann | **Mark-M. Bakran**

Department of Mechatronics, Center for Energy Technology (ZET), University of Bayreuth, Bayreuth, Germany

Correspondence
Lukas Bergmann, Department of Mechatronics, Center for Energy Technology (ZET), University of Bayreuth, Universitaetsstrasse 30, 95440 Bayreuth, Germany.
Email: Lukas.Bergmann@uni-bayreuth.de

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Abstract

This article presents the design and experimental validation of a novel semiconductor area optimised 3300 V half bridge with Silicon Carbide (SiC) MOSFETs for HVDC converters. Based on a loss simulation, the problem statement is provided. On this results, a mathematical derivation for the optimised semiconductor area design is executed. After this step, a system loss simulation shows the performance in efficiency and specific output power. Finally, a proof of concept was provided by a scaled hardware test setup to characterise the dynamic behaviour of the novel SiC half bridge design compared to the conventional SiC half bridge.

1 | INTRODUCTION

The benefits of using Modular Multilevel Converters (MMC) in HVDC applications has been discussed in many papers and in various MMC HVDC projects around the globe such as the *Transbay Project* in 2010 [1]. The performance of generating a high sinusoidal output voltage with low harmonic distortion, the ability of a black start, the full bidirectional active and reactive power flow and the good scalability are the main advantages of MMC based HVDC converters [2]. Nowadays, the state-of-the-art Silicon (Si) IGBT based submodules show a great performance considering power level and efficiency [3]. Nevertheless, the need for a further decrease of losses is important due to the use as a key component in energy transmission systems. The fast improvement of high voltage (HV) SiC MOSFETs considering increasing blocking voltage, low on resistance, lower switching losses and unipolar behaviour opens a new semiconductor technology for high power converters [4, 5]. Furthermore, various concepts for the freewheeling diodes were attending for higher SiC voltage classes [6, 7]. Further investigations seem to be promising as other research have shown on system and circuit level presented in [8–12] and [13]. A review of comparison of Si and SiC based MMC can be found in [14, 15]. A first idea of adapting the Si semiconductor area due to odd losses in a half bridge (HB) MMC was presented in [16]. The recent focus on SiC MOSFETs opens a new field for design optimisation methods. However, only fewer investigations about potential design optimisations of SiC MOSFETs within the application of HVDC MMC were done so far. Hence this work appoints a new degree of freedom to select the required semiconductor area in a SiC based HB for MMCs. This work includes results of [17] and [18], which were already published as conference papers by the author. In this work, a new second design target option for the SiC AHB is presented to increase the efficiency by reusing the saved semiconductor area of the HS chip.

2 | MOTIVATION AND PROBLEM STATEMENT

The use of HV SiC MOSFETs allows novel prospects of design optimisation. One of them is the optimum use of semiconductor area for a better fit of investment costs. Due to the unipolar character of the device without bipolar plasma except the body diode, a free choice of semiconductor area is only thermally limited compared to the state-of-the-art Si IGBT based submodules. Therefore, the benchmark application for this investigation was an MMC with SiC MOSFET based HB submodules as illustrated in Figure 1.

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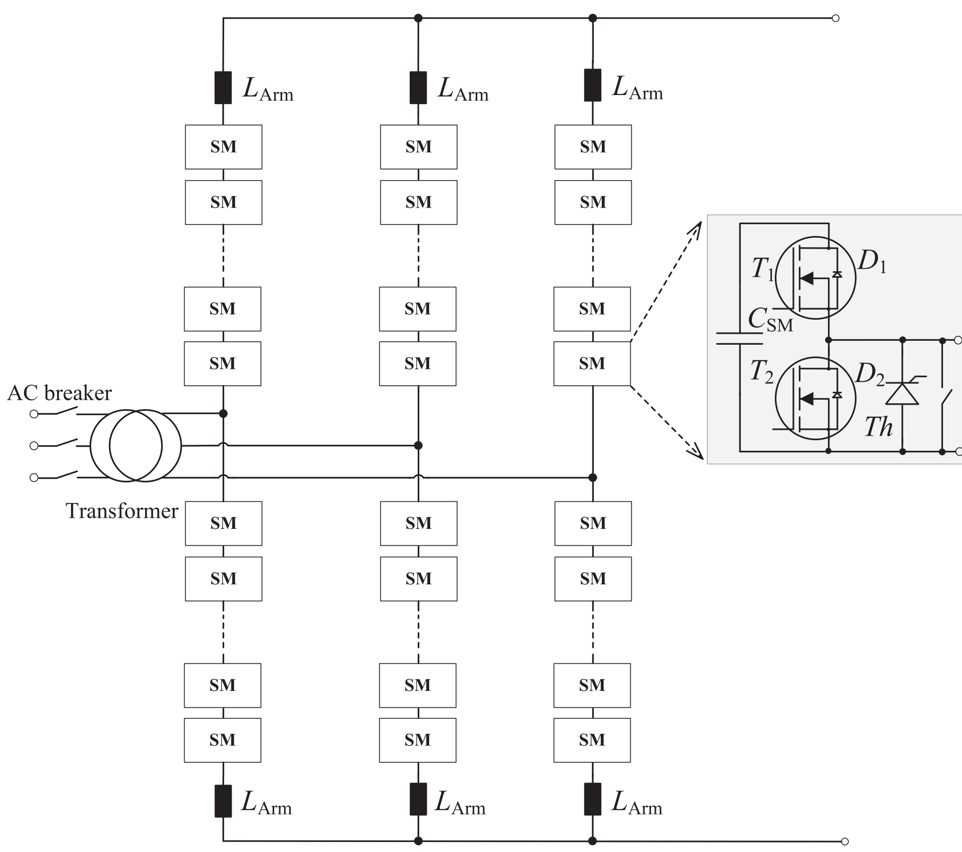

FIGURE 1 Investigated HVDC Converter: MMC with HV SiC MOSFET based HB submodules.

For all upcoming abbreviations, the low side (LS) switch corresponds to T2 whereas the high side (HS) switch to T1. All further abbreviations and symbols are listed in the appendix.

2.1 | Losses and junction temperature of conventional HB

The arm current i_{Arm} of an MMC consists of a sinusoidal AC and a DC part (Equation A1). This causes asymmetrical RMS values of the switching currents in the HB, which is illustrated in Figure 2.

Figure 3 shows the losses of the SHB in an MMC in the full range of converter DC current for rectifier $I_{DC} < 0$ and inverter $I_{DC} > 0$ operation. The simulation tool is based on the proposed loss model published in [19] and can be found in the appendix. A mostly linear forward and reverse conducting behaviour of the DUT leads to a parabola shape of the losses as proven in Figures A1 and A2. Furthermore, the most dominating losses in an SiC based HVDC MMC are conduction losses [20]. The maximum converter current is thermally limited to the first semiconductor component which will reach 125°C. The SHB shows a very odd utilization on the semiconductor HB components over the whole converter current operation. Obviously, the SHB has a high asymmetrical losses and temperature stress between the LS and HS devices within the HB (solid lines). This results in less T_J in the HS switch compared to the LS switch, which is equivalent to a very low utilization of the HS switch (Figure 4). The asymmetrical strain can be explained by the odd arm current, which creates asymmetrical RMS values as illustrated in Figure 2.

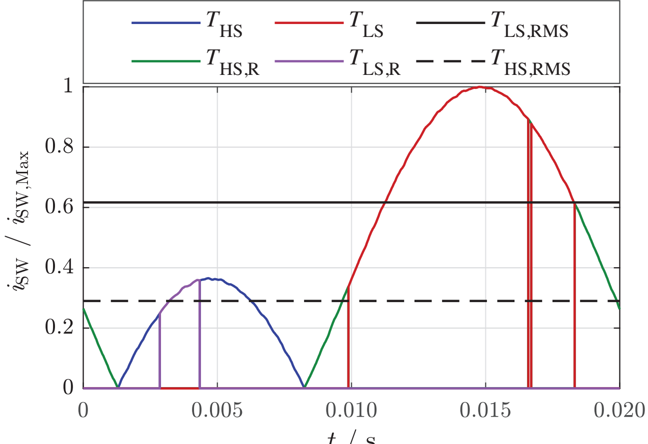

FIGURE 2 Envelope of forward and reverse (R) switching currents in LS and HS switch of a MMC HB submodule.

The subsequent T_J of the LS and HS switches for the SHB (solid lines) and the AHB (dotted) is shown in Figure 4. The LS temperature remains identical for both HB designs.

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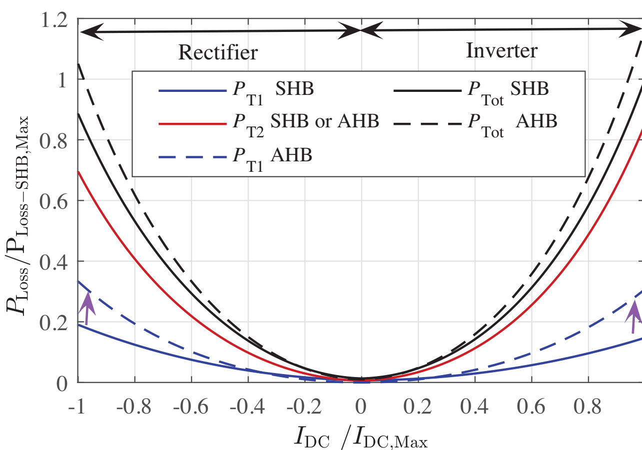

FIGURE 3 Comparison of total power losses for the SHB and the AHB half bridge with reduced HS area.

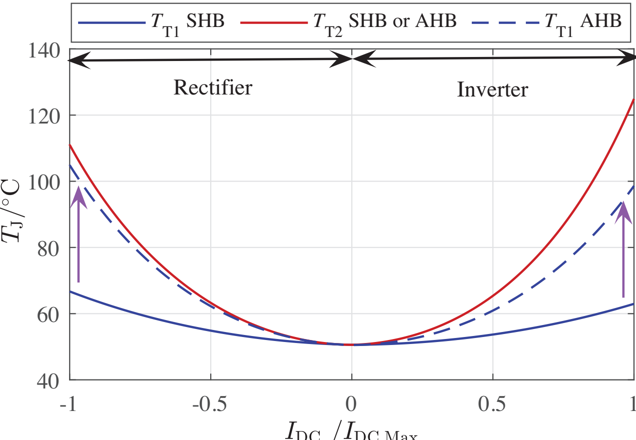

FIGURE 4 Comparison of T_J for the SHB and the AHB half bridge with reduced HS area.

2.2 | Mathematical derivation of the semiconductor area design pattern

For the design optimum of semiconductor area, the dependence of T_J by the semiconductor area has to be taken in account. No switching losses were considered in the derivation due to their minor role of total losses by 6% [20]. There are two major impacts on the T_J by the semiconductor area of LS and HS switch as shown in Equation (1).

$$\begin{aligned}\Delta T_{JC}(A_{Active}) &= R_{Th} \cdot R_{DSon} \cdot I_{RMS}^2 \\ &= r_{TH,JC} \cdot r_{DS,On} \cdot \frac{I_{RMS}^2}{A_{Active}^2}.\end{aligned} \tag{1}$$

The direct influence of semiconductor area on the electrical as well as the thermal resistance can be expressed by Equations (2) and (3).

$$R_{DS,On} = \frac{r_{DS,On}}{A_{Active}}, \tag{2}$$

$$R_{Th,JC} = \frac{r_{Th,JC}}{A_{Active}}. \tag{3}$$

This results in a second order dependency on T_J. Hence a HS to LS area ration (Equation 4) was defined, which expresses the ratio of HS and LS semiconductor area. All symbols are listed in the appendix.

$$a_{LSHSopt} := \frac{A'_{HS}}{A_{LS}} = \frac{A'_{HS}}{A_{HS}}. \tag{4}$$

The temperature lift of the novel AHB could be derived by Equation (5) depending on the effective current density $J_{HS,RMS}$ of the HS switch.

$$\begin{aligned}\Delta T'_{JC,HS}(A_{HS}) &= r_{TH,JC} \cdot r_{DS,On,HS} \cdot J_{HS,RMS}^2 \cdot \frac{1}{a_{LSHSopt}^2} \\ &= r_{TH,JC} \cdot \bar{p}_{Loss,SHB,HS}.\end{aligned} \tag{5}$$

The average power loss density per switch can be computed by Equation (6).

$$\bar{p}_{SHB} = \frac{1}{2 \cdot I_{DC,Max}} \cdot \int_{-I_{DC,Max}}^{+I_{DC,Max}} p_{SHB}\, dI_{DC}. \tag{6}$$

The same approach was used for the LS switch by Equation (7)

$$\begin{aligned}\Delta T_{JC,LS}(A_{LS}) &= r_{TH,JC} \cdot r_{DS,On,LS} \cdot J_{LS,RMS}^2 \\ &= r_{TH,JC} \cdot \bar{p}_{Loss,SHB,LS}.\end{aligned} \tag{7}$$

The conditions for both T_J must fulfilled by $\Delta T'_{JC,HS} \stackrel{!}{=} \Delta T_{JC,LS}$. By equal values for Equations (5) and (7), the following correlation was derived:

$$r_{TH,JC} \cdot \bar{p}_{Loss,SHB,HS} \frac{1}{a_{LSHSopt}^2} = r_{TH,JC} \cdot \bar{p}_{Loss,SHB,LS}.$$

Following the area design ratio was derived on the power loss density for the LS and HS switch by Equation (8).

$$a_{LSHS,opt} = \sqrt{\frac{\bar{p}_{Loss,SHB,HS}}{\bar{p}_{Loss,SHB,LS}}}. \tag{8}$$

3 | DESIGN TARGET OPTIONS FOR THE ASYMMETRICAL SiC HALF BRIDGE

In this section, the two basic target options are shown with respect to their pro and contra aspects. The first target option was a cost optimised version of the AHB with less total semiconductor area compared to the SHB. This version will save costly semiconductor area for the drawback of less system efficiency. The second target option was a reuse of semiconductor

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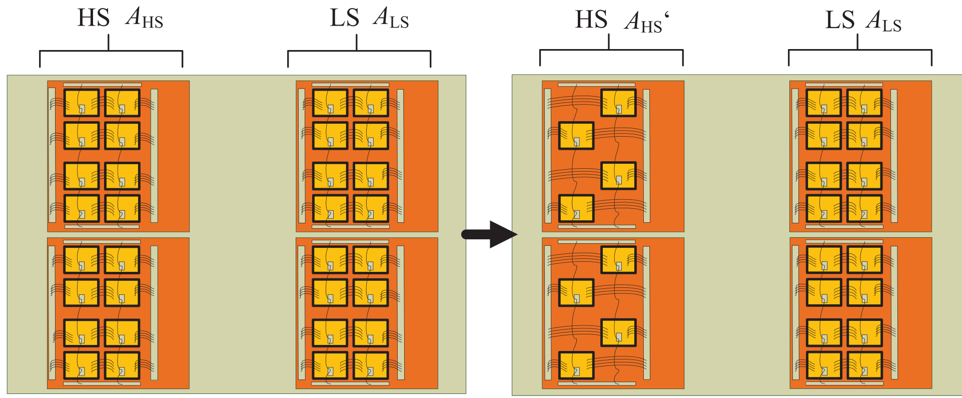

FIGURE 5 Example: Basic chip layout of conventional SHB (left) and semiconductor area reduced design AHB1 (right).

area from HS to LS for a further reduction of losses in the higher strained LS switch. In this case the semiconductor costs remain the same but a higher efficiency could be achieved compared to the SHB.

3.1 | Design target I: Reduction of total semiconductor area

The semiconductor ratio for AHB1 with a target option to reduce the total semiconductor area could be derived by Equation (8) with a value of $a_{\mathrm{LSHS,opt}} = \sqrt{\bar{p}_{\mathrm{Loss,SHB,HS}}/\bar{p}_{\mathrm{Loss,SHB,LS}}} = \sqrt{0.0734/0.2593} = 0.53.$ In this design, the number of chips for the conventional SiC HB was 16 chips per switch, which sums up to 32 chips for the total SiC HB module package. Therefore, a design proposal of 8 chips for the HS and 16 chips for the LS switch was made as illustrated in Figure 5. The final correctness to reach the optimum $a_{\mathrm{LSHS,opt}}$ in the real world application depends on the numbers of total chips per switch, which enables a higher resolution. The resulting efficiency for the AHB1 was 99.71% and therefore 0.04% less compared to the SiC SHB reference, which is illustrated by Figure 7. However, the efficiency was 0.07% higher compared to the Si IGBT based reference. The total semiconductor area of the AHB1 design was approx. 25% less compared to the SHB reference at an identical output power. Therefore, the design AHB1 design represents the fix costs reduced HB type.

3.2 | Design target II: Optimal reuse of total semiconductor area

The second design target with an optimum distribution of semiconductor area between LS and HS switch features also less semiconductor area in the HS compared to the LS switch (Figure 6). In this case, the reduced HS area is added to the LS switch which resulted in an identical total area for the whole SiC HB. The HS switch is reduced from 16 chips to 10 chips which is equivalent to a 37.5% reduction. The cut down HS area was added to the LS switch, which increased by 37.5%. In the example module, the number of LS chips was increased from 16 to 22. The total optimum area ratio from HS to LS remained almost the same as for the design of AHB1 with a ratio of $a_{\mathrm{LSHS,opt}} = 10/22 = 0.45$ compared to $8/16 = 0.50$. The second design target AHB2 reached an efficiency of 99.79%. For the AHB2 the total semiconductor area remained the same like the SHB. Therefore, the All SiC designs showed a better efficiency compared to the Si reference design as illustrated in Figure 7.

TABLE 1 Measurement conditions and basic DUT information.

Type	Value/specifications
Oscilloscope	LeCroy, 12-bit, WaveRunner 8108HD
HV-probes	PMK 641-L, 100:1, 380 MHz
Current measurement	CWT / 6 / R, 1.2 kA
FOB probes	LeCroy HVFO108 (HS gate voltages)
DUT	3.3 kV SiC MOSFET, $I_{\mathrm{Nom}} = 45$ A
Gate voltage levels	$V_{\mathrm{GS}} = -5$ V/ + 17 V
Internal gate resistor	30 Ω
Stray inductance	1500 nH for both HB types
Load inductance	5 mH
DC cell voltage	$V_{\mathrm{Cell}} = 1800$ V
Case temperatures	25° C for cold and 125° C for hot tests

4 | EXPERIMENTAL VALIDATION

The last section focuses on the experimental validation by a characterisation of the switching behaviour. First, the experimental method is described. Furthermore, the hardware setup and basic circuit typologies are illustrated. Finally, the experimental results with respect to various dynamic parameters are presented. In this case, only the AHB1 is compared to the SHB due to the easy scaling with discrete devices. As the semiconductor ratio of LS and HS for the AHB1 and AHB2 is the same, the basic results are valid for both AHB designs. The measurement condition and basic DUT information is listed in Table 1. A picture of the hardware test setup is visualised in Figure 8.

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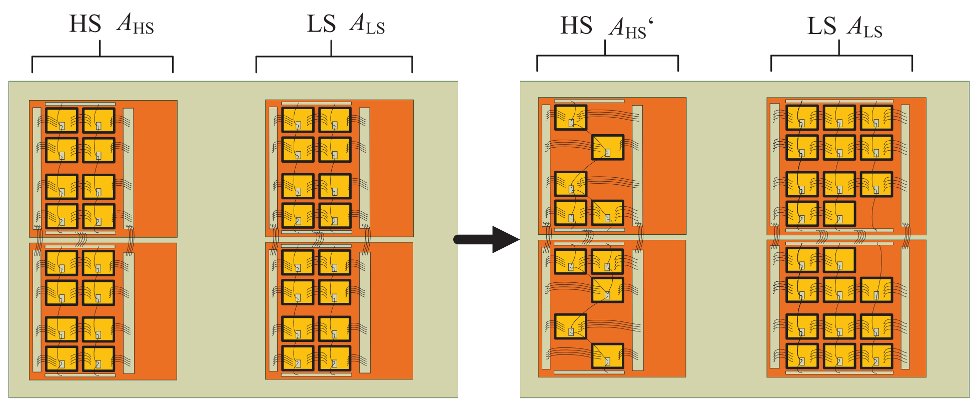

FIGURE 6 Example: Basic chip layout of conventional SHB (left) and semiconductor area optimum distributed design AHB2 (right).

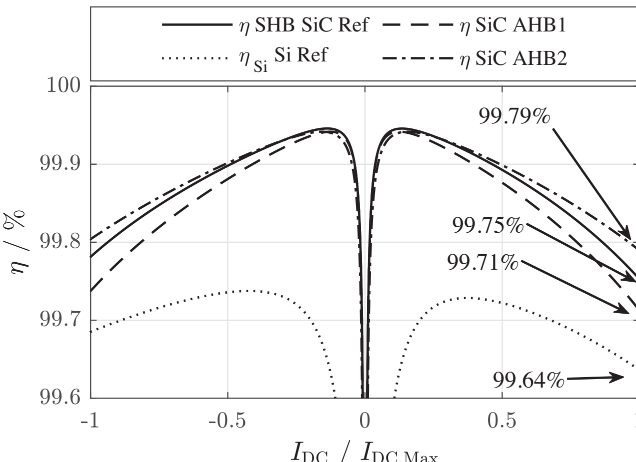

FIGURE 7 System efficiency of converter for both AHB design targets, SiC SHB reference and Si reference for identical converter power.

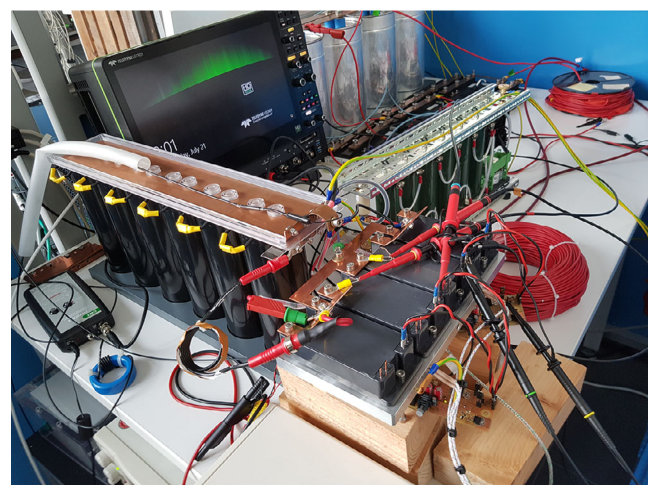

FIGURE 8 Photograph of the hardware test setup (Example of SHB).

4.1 | Circuit topologies and hardware test setup

The submodule cells of a state-of-the-art HVDC MMC consists of the submodule capacitor, the busbar and the semiconductor power modules with multiple chips in parallel. To avoid unnecessary expenses and demands, a scaled hardware test setup with discrete 3.3 kV SiC MOSFETs was used. The SHB was realised by two single chip based parallel half bridges as illustrated in Figure 9. This setup of the SHB was also used as fair reference for the AHB, which consists of 50% less HS semiconductor area by removing one chip of the HS switch (Figure 10).

The experimental validation for both HB types was executed by a double pulse test setup (Figure A4). The parameters for characterisation were scaled values from an SiC HB power module of the real application to discrete chips. The values are shown in Table 1.

The subsequent subsections focus on the anomalies of switching characteristics, gate resistor design and freewheeling diode operation between the SHB and AHB. A deeper look on the anomalies of switching, gate resistor design and dead time optimisation between the LS and HS components of the AHB will conclude this section.

For all tests, an identical stray inductance of 1500 nH was applied as shown in Table 1. This value is equivalent to a power module with 16 chips. For a better visibility of the traces, all current values are multiplied by a factor of ten.

4.2 | Turn-off switching comparison of both HB types

The turn-off switching characterisation was executed at T_J = 25° C. For both HB types, the LS and HS switches were characterised. The external turn off gate resistors $R_{G,Off}$ were designed to reach a maximum turn off voltage of 600 V at 137.5 A additionally to the DC link voltage. The total sum would be 2400 V with 1800 V DC link voltage. This value would correspond to 3000 V at a 2400 V DC link voltage, which is the maximum voltage level before a pulse stop in a 3.3 kV MMC submodule.

The maximum switching current of 137.5 A corresponds to 1100 A for a power module with 16 chips, as the test setup contains two chips in parallel. The $R_{G,Off}$ design was straightforward. Thus, the doubled semiconductor area switches get half valued as a common $R_{G,Off}$ compared to the HS single chip. For the LS turn-off switching, the experiment showed

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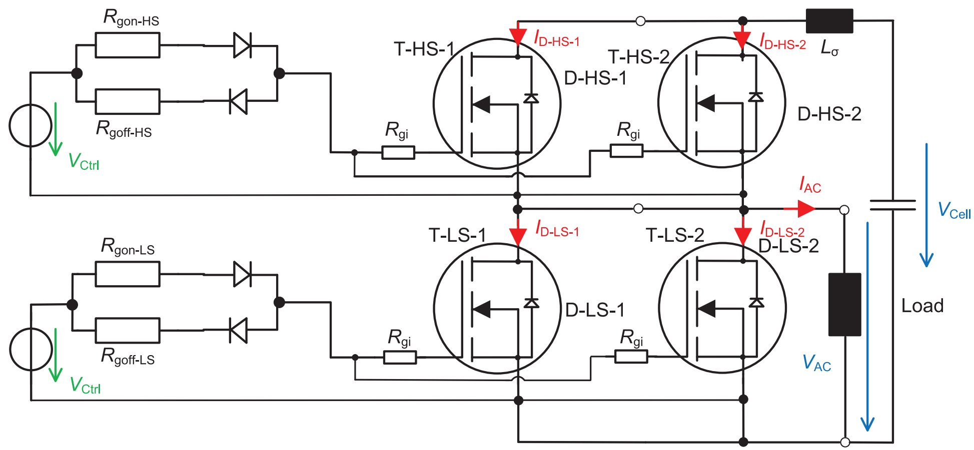

FIGURE 9 Basic circuit typology of conventional SiC SHB as reference.

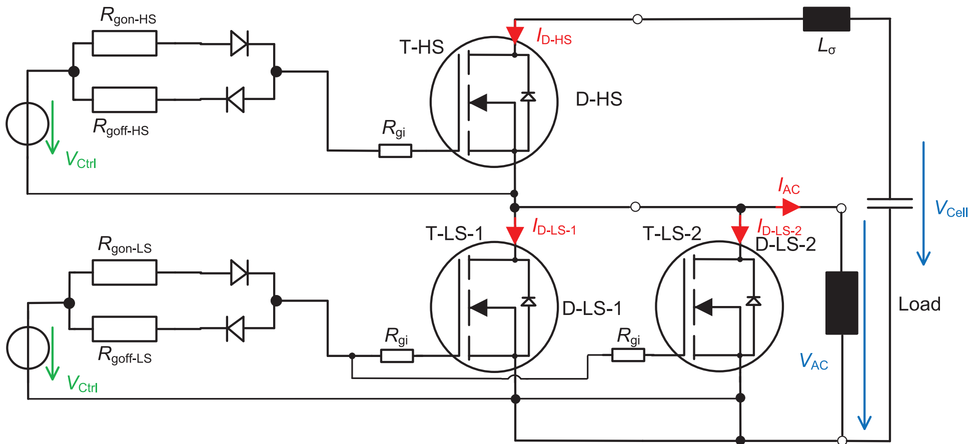

FIGURE 10 Basic circuit typology for the hardware test setup of the novel SiC AHB.

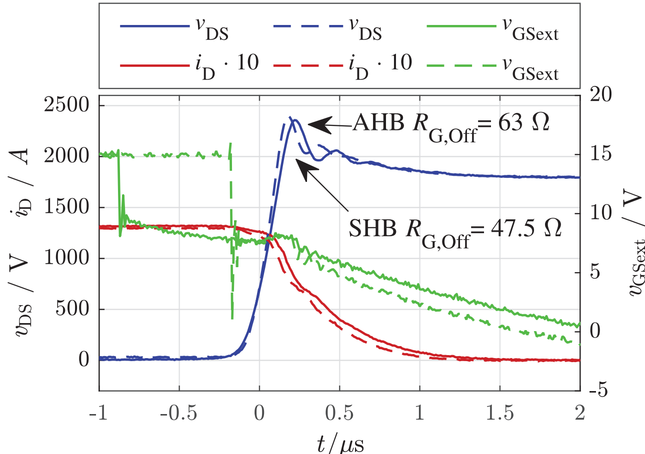

FIGURE 11 HS switch turn-off characteristics of both HB types, HS switch SHB (solid), HS switch AHB (dashed).

identical results for both HB types as the semiconductor area was identical. Therefore, only the HS switching characteristics are illustrated within this paper in Figure 11. The SHB consists of two paralleled HS chips and therefore both share an equivalent current of half of the total switching current if there is no current mismatch. The pinch-off voltage is increased at higher currents for the AHB HS switch at identical current, which is illustrated in the different transfer characteristics in Figure 12. The fall time is increasing and therefore the absolute value of *didt* would decrease. Thus the absolute *didt* of one chip is slower compared to two paralleled chips when using identical gate resistance per chip and switching off a current of 137.5 A. The slower *didt* of a single chip at identical current results in a lower overshoot switch-off voltage of V_{DS} is shown in Figure 13. Consequently $R_{G,Off}$ can be decreased to reach the identical turn-off voltage. This effect explains why $R_{G,Off}$ of the AHB is 63 Ω instead of 95 Ω, which would be the straightforward design, as it marks the doubled value of 47.5 Ω. The internal gate resistance $R_{G,i}$ of 30 Ω is added additionally for each chip of the HB types. Thus, the total gate resistance per chip was reduced from 125 Ω to 93 Ω for the AHB, which is equivalent of a reduction by 25%. The total turn-off losses E_{Off} are decreased from 103 mJ to 87 mJ at the full current of 137.5 A (Figure 14). A second side effect besides a lower E_{Off} was the decreased effective output capacitance of one chip compared to two chips. In this subsection, the HS switch off characteristics were investigated for both HB types. There was a proof of concept by experimental

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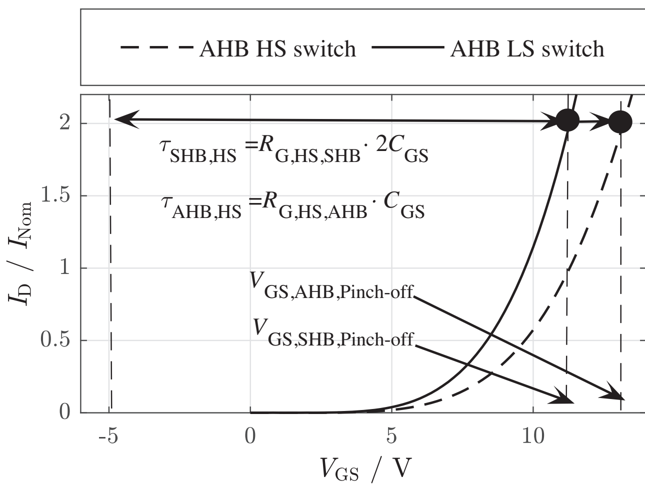

FIGURE 12 Transfer characteristics and pinch-off voltage at $2 \cdot I_{Nom}$ for HS switch SHB (solid) vs. HS switch AHB (dashed).

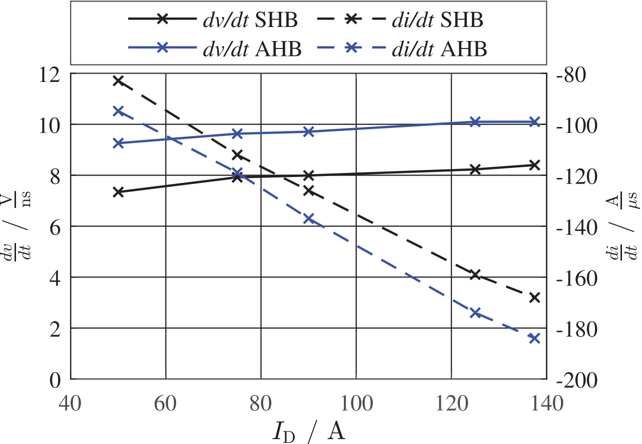

FIGURE 13 Voltage and current turn-off slopes of both HB types.

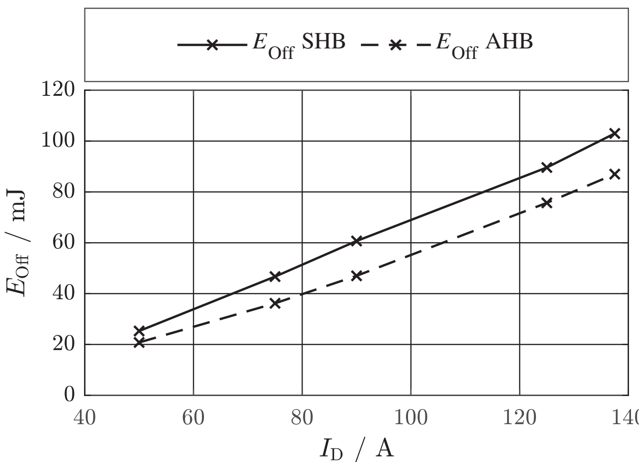

FIGURE 14 HS switch turn-off losses of both HB types, HS switch SHB (solid), HS switch SHB (dashed).

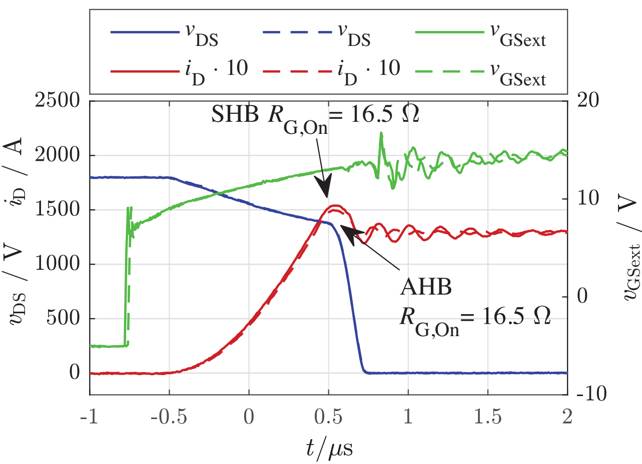

FIGURE 15 LS switch turn-on characteristics of both HB types.

validation and how to design the corresponding external $R_{G,Off}$. Even with the 50% reduced HS switch semiconductor area, the turn-off switching characteristics of the AHB shows only minor differences compared to the conventional HB.

4.3 | Turn-on switching comparison of both HB types

In this subsection, both HB types were investigated for the turn on characteristics of the LS and HS switch. Both LS and HS switch were tested in an active switch role. Additionally, the complementary freewheeling body diodes were characterised for their turn off behaviour. The value of $R_{G,On}$ was adjusted to achieve a maximum turn off voltage of 600 V for the body diodes at maximum switching current and junction temperature of 125°C. No parallel reverse conducting channel was used to support the freewheeling diodes with synchronous rectifying. Therefore, the gate voltage V_{GS} was tuned to −5 V for the passive switches.

The first approach was to select identical $R_{G,On}$ as the LS chip of both HB types as illustrated in Figures 9 and 10. However, the HS body diode of the AHB showed a lower turn voltage peak for the identical switching current as it featured less semiconductor area. The comparison of turn on of both active switches is shown in Figure 15. The maximum diode turn off voltage was 500 V for the AHB and 670 V for the SHB (Figure 16). This effect could be explained by the higher semiconductor area of SHB which leads to more reverse recovery charge Q_{RR} at an identical bipolar current. This investigation revealed the more dominant impact of the semiconductor area on Q_{RR} and is illustrated in Figure 19.

The straightforward design of the LS $R_{G,On}$ design was feasible for both Hb types as the turn off voltages of the body diodes showed only minor variances as illustrated in Figure 16. The turn on transients over the various switching currents showed also similar values as illustrated in Figure 17. Consequently, the LS turn on losses E_{On} as well as the diode losses E_{RR} had only minor differences which is presented in Figure 18. The

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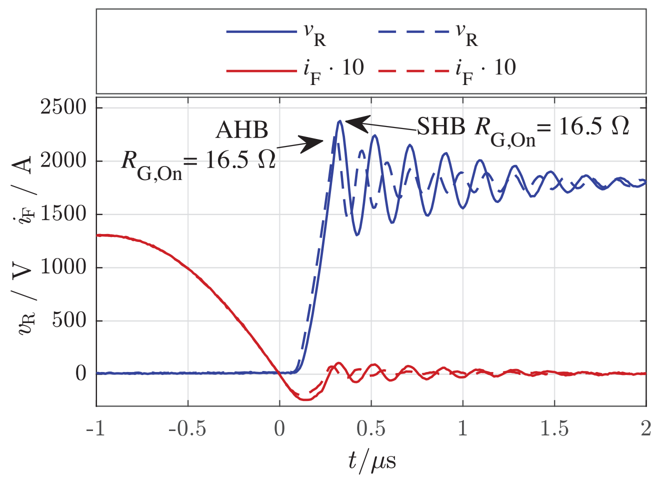

FIGURE 16 Corresponding HS Body diode turn-off characteristics of both HB types.

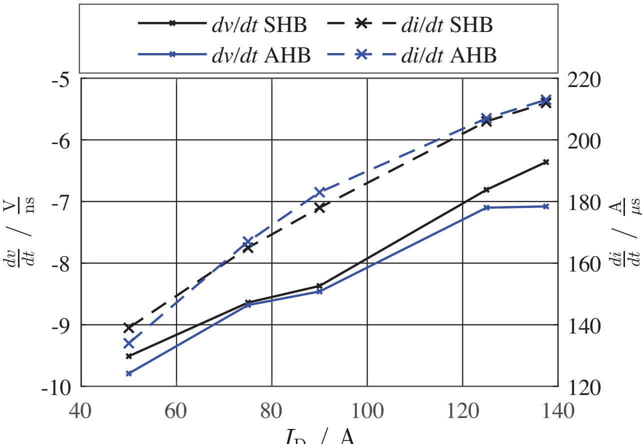

FIGURE 17 Voltage and current turn-on slopes of both HB types.

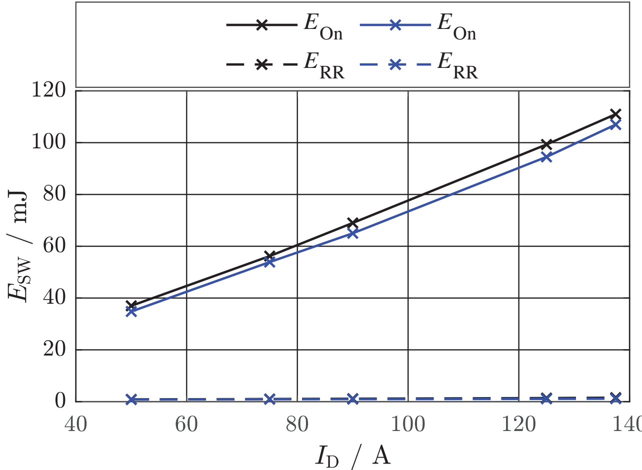

FIGURE 18 LS switch turn-on losses of both HB types, SHB (black), AHB (blue).

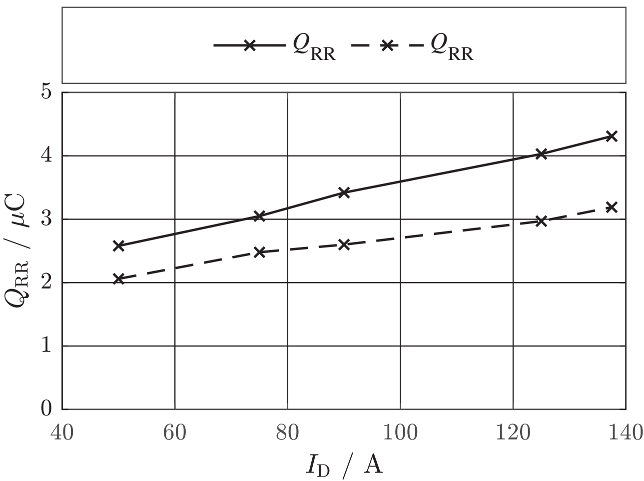

FIGURE 19 Corresponding HS Body diodes Q_{RR} over current, SHB (solid), AHB (dashed).

comparison of Q_{RR} for both HB types is shown in Figure 19. These curves reveal that the SHB semiconductor area of the bipolar body diode with a shared switching current generates more bipolar charge compared to the half semiconductor area of the AHB with the identical current. Additionally, more capacitive charge is generated by the doubled semiconductor area. For the AHB body diode, the reverse recovery charge Q_{RR} was approximately 25% less than the SHB HS body diodes. The overall straightforward design for the turn on control of the LS switches was possible for both HB types to achieve a similar switching behaviour for the active and passive switches.

4.4 | Comparison of the AHB LS vs. AHB HS switch

The asymmetrical semiconductor area of the LS and HS switch within the AHB is evaluated in this subsection with regard to the active turn on and body diode switching behaviour. The straight-forward design for $R_{G,On}$ was chosen for the LS and HS switch which led to an almost similar turn on characteristic as illustrated in Figure 20. The turn off switching of the complementary body diodes indicated also a very similar switching behaviour (Figure 21). It should be noted that the total effective gate-on resistor value per chip is a sum of the internal gate resistance $R_{G,int}$ per chip and $R_{G,On}$ per chip. The effective external $R_{G,On}$ of one chip is determined by the common driver path between driver voltage and common gate-on path of the parallel devices. Thus, the total turn on RC time constant of the LS switches is double the value of the HS switch time constant. Since $R_{G,int}$ is 30 Ω, the external $R_{G,On}$ of the HS switch was selected to 0 Ω for achieving the same over-shoot voltage as the corresponding LS body diodes. For the LS switches, $R_{G,int}$ of the common driver was tuned to 16.5 Ω. So in each chip gate path of the parallel LS switches, a total effective gate-on value of 46.5 Ω appears. The HS switch had an effective value of 30 Ω

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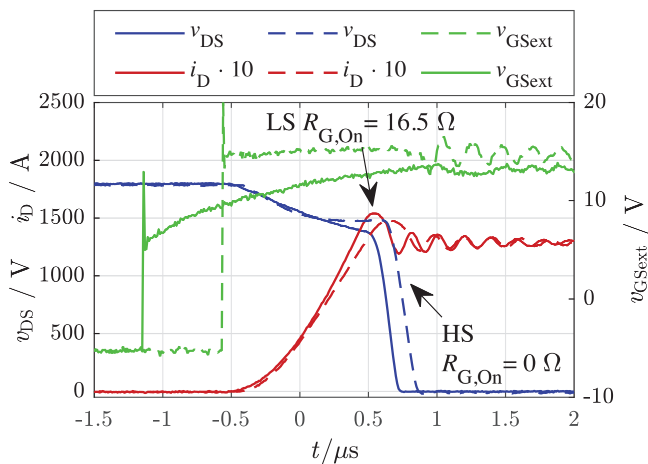

FIGURE 20 LS and HS turn-on switching of AHB, LS switch (solid lines), HS switch (dashed lines).

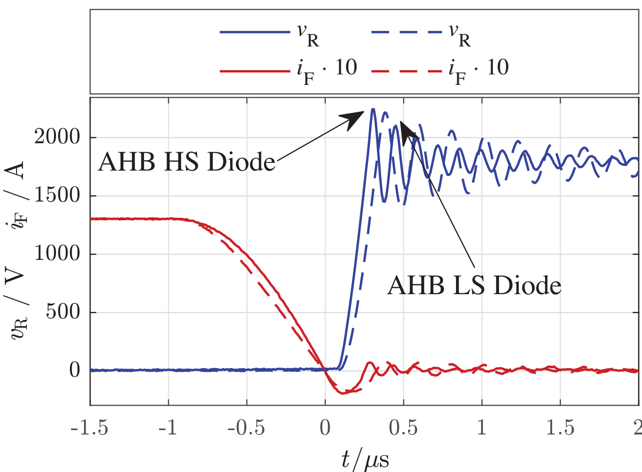

FIGURE 21 LS and HS body diode turn-off switching of AHB, LS diode (dashed lines), HS diode (solid lines).

as the external $R_{G,On}$ was 0 **Ω**. Also, in this case the odd values can be explained by the higher pinch-off voltage of a single chip conducting the identical current compared to two chips in parallel (Figure 12). The oscillations of the HS diode turn-off voltage showed a higher frequency as the output capacitances of the HS switch is half of the LS switch. Also for this case, almost identical switching characteristics were achieved for the LS and HS switch of the AHB.

4.5 | Influence of interlock time optimisation on AHB

The interlock time also defined dead time T_{Dead} as the conducting time of the body diode of the passive switch between the conducting of active and reverse conducting passive switch (Figures A3 and A5). The basic influence of interlock time on the switching characteristic of the body diode was already investigated in [20] and [21]. Therefore, only the result of interlock time optimisation for the new design is presented. It is executed

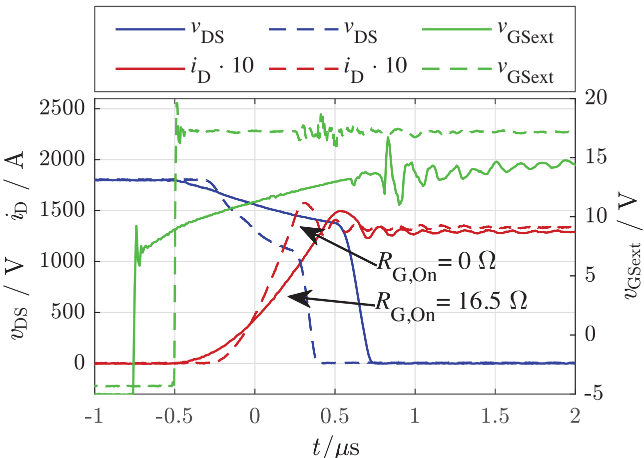

FIGURE 22 Influence of T_{Dead} on turn-on switching of the AHB, AHB no opt. $T_{Dead} \geq 5$ ¯s (solid), AHB w. $T_{Dashed} = 1.5$ ¯s (dashed).

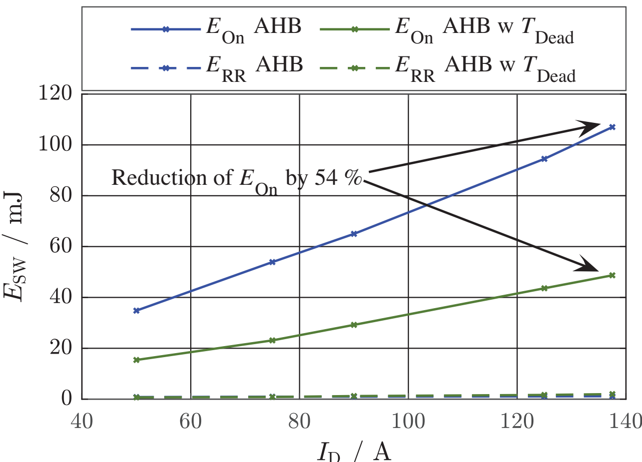

FIGURE 23 Influence of T_{Dead} optimisation on turn-on losses, AHB no opt. $T_{Dead} \geq 5$ ¯s (blue), AHB w. $T_{Dead} = 1.5$ ¯s (green).

in multiple iteration steps. The first step is a decreasing of T_{Dead} until a bridge short circuit occurs between LS and HS switches. The last good value before the short circuit event determines the optimised T_{Dead} at a given $R_{G,On}$ at the maximum switching current. The second step of the iteration process is a reduction of $R_{G,On}$ until the maximum diode turn off voltage occurs. Now the iteration loop of decreasing T_{Dead} starts again until the minimum possible $R_{G,On}$ is reached.

The reduced turn off voltage in the freewheeling diode allows the user to decrease the external $R_{G,On}$ of the active switch to even 0 **Ω** (Figure 22). The faster turn on events lead to less E_{On}. Finally, E_{On} could be reduced by 54% leading from 107 mJ to 46 mJ at maximum switching current (Figure 23). A $R_{G,int}$ of 30 **Ω** and a T_{Dead} of 1.5 μs induced an almost identical diode turn off voltage as that without any reverse channel conduction of the HS switch (Figure 24). The total Q_{RR} was reduced from 3.2 ¯C to 2.6 ¯C which is a relative reduction by 19%. This subsection focused on the impact of an optimum T_{Dead} on the AHB. It was demonstrated that the choice of an optimum T_{Dead} is also useful to reduce the Q_{RR} (Figure 25) and

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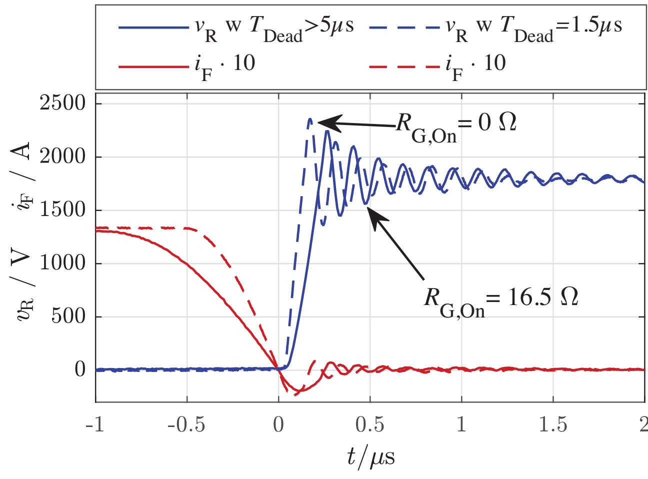

FIGURE 24 Influence of T_{Dead} on dynamic characteristics of the body diode, no opt T_{Dead} (solid), w T_{Dead} (dashed).

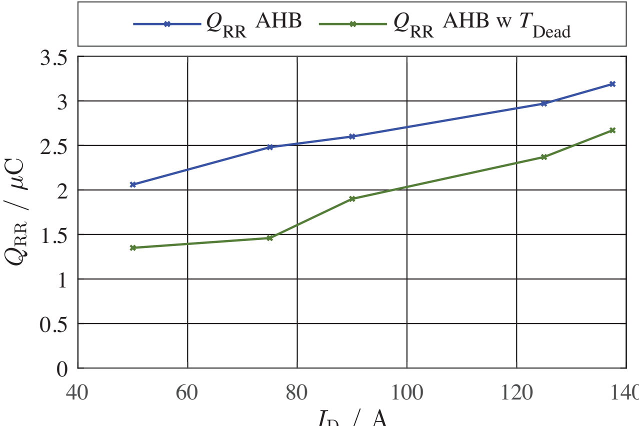

FIGURE 25 Influence of T_{Dead} optimisation on Q_{RR}, AHB HS no opt. $T_{Dead} \geq 5$ ¯s (blue), AHB HS w. $T_{Dead} = 1.5$ ¯s (green).

therefore decrease the turn-on switching losses by a reduced gate resistor design.

4.6 | Overview external gate resistance design

This final subsection will sum up the final gate resistor values which were used for both HB types and aims to provide an overview to design the AHB. All values are listed in Table 2. The beginning subsection discussed the turn off switching of the AHB. After this, two different turn on event cases were investigated in the previous subsections. First, the turn-on switching without any reverse conducting MOSFET channel to the parallel freewheeling body diode. Secondly, the activation of the reverse conducting MOSFET channel with an optimised dead time. At a first glance, the adjustment of identical time constant values τ_G was not successful for a similar switching event due to the modified transfer characteristics of one compared to two chips. Therefore, the time constant of the HS switch $\tau_{AHB,HS}$ had to be further reduced for the identical switching speed.

TABLE 2 Overview of external gate resistor design for all switches.

Switch	Value	
LS SHB $R_{G,Off}$	47.5 Ω	
HS SHB $R_{G,Off}$	47.5 Ω	
LS AHB $R_{G,Off}$	47.5 Ω	
HS AHB $R_{G,Off}$	63 Ω	
LS SHB $R_{G,On}$	16.5 Ω ($T_{Dead} \geq 5\ \mu s$)	0 Ω ($T_{Dead} = 1.5\ \mu s$)
HS SHB $R_{G,On}$	16.5 Ω ($T_{Dead} \geq 5\ \mu s$)	0 Ω ($T_{Dead} = 1.5\ \mu s$)
LS AHB $R_{G,On}$	16.5 Ω ($T_{Dead} \geq 5\ \mu s$)	0 Ω ($T_{Dead} = 1.5\ \mu s$)
HS AHB $R_{G,On}$	0 Ω ($T_{Dead} \geq 5\ \mu s$)	0 Ω ($T_{Dead} = 1.5\ \mu s$)

4.7 | Discussion and outlook

This investigation of the AHB design was based on simulation for system evaluation, whereas the critical switching cell design was validated by an experimental hardware test for 3.3 kV SiC MOSFET devices. Further research focuses on higher voltages classes such as 6.5 kV SiC devices, which will also be investigated for the novel AHB design approach. A comparison of MMC submodule voltage classes for 3.3 kV and 6.5 kV SiC SHBs was already executed in [22]. Another interesting topic would be a scaled MMC hardware platform equipped with the novel AHB to evaluate the benefits on system level by a complete converter hardware platform.

5 | CONCLUSION

In this work, a novel design of a semiconductor area optimised 3.3 kV SiC HB for HVDC MMC submodules was introduced. The design rules for an optimised semiconductor area between the HS and the LS switch were derived from a mathematical derivation based on fundamental equations of electrical and thermal parameters. The design rules were validated by an MMC HB simulation tool for two different design targets. The AHB1 features a cost effective approach to save SiC chip costs with the drawback of less system efficiency whereas the AHB2 focuses on a more efficient distribution of the total semiconductor area to increase the efficiency. Finally, an experimental validation for switching characteristics of the novel HB design was executed. For this purpose, two discrete 3.3 kV SiC half bridge designs were validated in double pulse tests for switching performance. The first was the SHB as reference to the second HB which featured the AHB. A proof of concept was shown considering the optimal gate resistance design for the AHB. An almost identical switching behaviour was achieved by selecting proper gate resistors. The focus was on different effects of the reduced HS body diode capability considering reverse recovery charge, switching losses and overshoot voltage of the SiC MOSFET devices in the novel AHB design. The AHB has even less switching losses compared to the conventional SHB. Therefore, the use of an SiC AHB is possible to operate by choice of a proper gate resistor design. However, the final choice of use will depend on the ratio of converter fix costs and the economical loss costs of the system [23].

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AUTHOR CONTRIBUTIONS

Lukas Bergmann: Conceptualization; data curation; formal analysis; investigation; methodology; validation; visualization; writing—original draft; writing—review and editing. **Mark—M. Bakran**: Funding acquisition; resources; supervision.

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CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

ORCID

Lukas Bergmann https://orcid.org/0000-0002-7907-5990
Mark-M. Bakran https://orcid.org/0000-0002-0622-5855

REFERENCES

1. Dorn, J., Gambach, H., Strauss, J., Westerweller, T., Alligan, J.: Trans Bay Cable – A Breakthrough of VSC Multilevel Converters in HVDC Transmission. Cigre, San Francisco (2010)
2. Raju, M., Sreedevi, J., Mandi, R., Meera, K.S.: Modular multilevel converters technology: a comprehensive study on its topologies, modelling, control and applications. IET Power Electron. 12(2), 149–169 (2019)
3. Marquardt, R.: Modular multilevel converters: State of the art and future progress. IEEE Power Electron. Mag. 5(4), 24–31 (2018)
4. Palmour, J.W., Cheng, L., Pala, V., Brunt, E.V., Lichtenwalner, D.J., Wang, G.-Y., Richmond, J., O'Loughlin, M., Ryu, S., Allen, S.T., Burk, A.A.: Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV. In: 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 79–82. IEEE, Piscataway (2014)
5. Nakashima, J., Fukumoto, A., Obiraki, Y., Oi, T., Mitsui, Y., Nakatake, H., Toyoda, Y., Nishizawa, A., Kawahara, K., Hino, S., Watanabe, H., Negishi, T., Iura, S.: 6.5-kV Full SiC power module (HV100) with SBD-embedded SiC MOSFETs. In: PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1–7. IEEE, Piscataway (2018)
6. Kawahara, K., Hino, S., Sadamatsu, K., Nakao, Y., Iwamatsu, T., Nakata, S., Tomohisa, S., Yamakawa, S.: Impact of embedding Schottky barrier diodes into 3.3 kV and 6.5 kV SiC MOSFETs. Mat. Sc. Forum 924, 663–666 (2018)
7. Tominaga, T., Hino, S., Mitsui, Y., Nakashima, J., Kawahara, K., Tomohisa, S., Miura, N.: Superior Switching Characteristics of SiC-MOSFET Embedding SBD. In: 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 27–30. IEEE, Piscataway (2019)
8. Hohmann, F., Bakran, M.-M.: Applying a 3300V SiC half-bridge to an MMC based HVDC system. In: 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), pp. 1–9. IEEE, Piscataway (2019)
9. Huang, X., Ji, S., Li, D., Nie, C., Giewont, W., Tolbert, L.M., Wang, F.: A Test Scheme for the Comprehensive Qualification of MMC Submodule Based on 10 kV SiC MOSFETs under High dv/dt. In: 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), pp. P.1–P.10. Lyon, France (2020)
10. Ishii, Y., Jimichi, T.: Verification of SiC based modular multilevel cascade converter (MMCC) for HVDC transmission systems. In: 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), pp. 1834–1839. IEEE, Piscataway (2018)
11. Jianghui, Y., Burgos, R., Mehrabadi, N.R., Boroyevich, D.: Design of a SiC-Based Modular Multilevel Converter for medium dc distribution system. In: 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 467–473. IEEE, Piscataway (2017)
12. Dahmen, C., Marquardt, R.: Power losses of advanced MMC submodule topologies using Si- and SiC-semiconductors. In: 21st European Conference on Power Electronics and Applications (EPE), pp. 1–10. IEEE, Piscataway (2019)
13. Zhang, S., Sun, L., Xue, X., Lv, H., Jia, R.: An SiC-based soft-switching and self-power supply MMC for MVDC. IET Power Electron. 16(10), 1649–1666 (2023)
14. Jacobs, K., Heinig, S., Johannesson, D., Norrga, S., Nee, H.-P.: Comparative evaluation of voltage source converters with silicon carbide semiconductor devices for high-voltage direct current transmission HVDC converters. IEEE Trans. Power Electron. 36(8), 8887–8906 (2021)
15. Jacobs, K.: Silicon-carbide-based high-voltage submodules for HVDC voltage-source converters. PhD Thesis, KTH Royal Institute Of Technology (2020)
16. Eckel, H.-G., Runge, J.: Comparison of the semiconductor losses in self commutated inverter topologies for HVDC. In: Proceedings of the 2011 14th European Conference on Power Electronics and Applications, pp. 1–8. IEEE, Piscataway (2011)
17. Bergmann, L., Wahle, M., Bakran, M.-M.: Optimization of the chip area in 3.3 kV SiC submodules for HVDC converters. In: 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), pp. 1–10. IEEE, Piscataway (2021)
18. Bergmann, L., Wahle, M., Bakran, M.-M.: Experimental validation of a chip area optimized 3.3 kV SiC half bridge for HVDC converters. In: 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1645–1652. IEEE, Piscataway (2022)
19. Schoen, A., Birkel, A., Bakran, M.-M.: Modulation and losses of modular multilevel converters for HVDC applications. In: Power Electronics, Intelligent Motion, Renewable Energy, and Energy Management (PCIM), pp. 1348–1355. IEEE, Piscataway (2014)
20. Horff, R., Maerz, A., Bakran, M.-M.: Analysis of reverse-recovery behaviour of SiC MOSFET body-diode—Regarding dead-time. In: Power Electronics, Intelligent Motion, Renewable Energy, and Energy Management (PCIM), pp. 1114–1121. IEEE, Piscataway (2015)
21. Liu, X., Li, X., Herrmann, C., Basler, T.: The impact of the dead-time on the reverse recovery behavior of SiC-MOSFET body diodes. In: Proc. 35th Int. Symp. on Pow. Semicond. Dev. and ICs, pp. 322–325. IEEE, Piscataway (2023)
22. Bergmann, L., Wahle, M., Bakran, M.-M.: Voltage class comparison of 3.3 kV SiC and 6.5 kV SiC devices in the application of HVDC converters. In: 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), pp. 1–10. IEEE, Piscataway (2023)
23. Ganesh, G., Patro, S., Chaturvedi, P.: SiC-based MMC for HVDC applications: A cost-benefit analysis. In: 2022 IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation (SeFeT), pp. 1–6. IEEE, Piscataway (2022)

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APPENDIX

Symbol	Explanation/comment
ΔT_{JC}	Rise of junction temperate from junction to case
A_{Active}	Active chip semiconductor area without edge termination
SHB / AHB	Symmetrical / Asymmetrical half bridge
$A_{LS/HS}$	Active chip semiconductor area of LS / HS switch
A'_{HS}	Reduced active chip semiconductor area of HS switch in AHB
$a_{LSHS,opt}$	Semiconductor area design ratio from HS to LS switch
δ	Ideal duty cycle of submodule modulator
η	Converter system efficiency: $\eta = 1 - (3 \cdot Ptot \cdot N)/P_{DC}$
f_{Out}	Average AC output frequency
f_{SW}	Average submodule switching frequency
I_{DC}	DC current of converter
$I_{LS/HS,RMS}$	Current RMS value of LS / HS switch
$J_{LS,RMS}$	Current density RMS value of LS switch
K_S	Redundancy factor of submodules
M	Modulation index $M = 2\hat{V}_{AC}/V_{DC}$
ϕ_I	AC load angle of converter
p_{SHB}	Power loss density of switch over DC current operation
P_{DC}	Total converter DC power $P_{DC} = V_{DC} \cdot I_{DC}$
$\bar{p}_{SHB}$	Average power loss density of switch over DC current operation
$R_{DS,On}$	Absolute conduction resistance of SiC MOSFET
$R_{TH,JC}$	Absolute thermal junction to case resistance
$r_{DS,On}$	Relative area specific conduction resistance of SiC MOSFET
$r_{TH,JC}$	Relative area specific thermal junction to case resistance
$R_{G,On/Off}$	External turn on / off gate resistor
T_{Dead}	Interlock dead time between LS und HS driver control signal
$\hat{V}_{AC}$	Peak value of converter AC output voltage
V_{DC}	DC link voltage of converter

Mathematical average loss model of MMC half bridge

$$i_{Arm}(t) = \frac{I_{DC}}{3} \cdot \left(1 - \frac{\sqrt{3} \cdot sin(\omega t - \phi_I)}{M \cdot cos(\phi_I)}\right), \tag{A1}$$

$$i_{Arm,pos} \text{ for } i_{Arm} \geq 0, \; i_{Arm,neg} = |i_{Arm} < 0|$$

$$\delta(t) = \frac{\pi \cdot M}{K_S(1+M)} \cdot \frac{2}{\sqrt{3}} \cdot \left(cos(\omega t) + \frac{1}{2} cos(3\omega t)\right), \tag{A2}$$

$$\Gamma = \frac{f_{SW}}{f_{Out}}, \; \Upsilon_{insert}(t) = \Gamma + \delta(t), \; \Upsilon_{bypass}(t) = \Gamma - \delta(t)$$

$$P_{C,HS} = \frac{1}{T} \cdot \int_0^T \delta \cdot v_{DS}(i_{Arm,neg}) \cdot i_{Arm,neg} dt, \tag{A3}$$

$$P_{C,HS,R} = \frac{1}{T} \cdot \int_0^T \delta \cdot v_{SD}(i_{Arm,pos}) \cdot i_{Arm,pos} dt, \tag{A4}$$

$$P_{C,LS} = \frac{1}{T} \cdot \int_0^T (1-\delta) \cdot v_{DS}(i_{Arm,pos}) \cdot i_{Arm,pos} dt, \tag{A5}$$

$$P_{C,LS,R} = \frac{1}{T} \cdot \int_0^T (1-\delta) \cdot v_{SD}(i_{Arm,neg}) \cdot i_{Arm,neg} dt, \tag{A6}$$

$$P_{SW,HS} = \frac{1}{T} \cdot \int_0^T (\Upsilon_{insert} \cdot E_{On}(i_{Arm,neg}) + \Upsilon_{bypass} \cdot E_{Off}(i_{Arm,neg}))dt, \tag{A7}$$

$$P_{SW,HS,D} = \frac{1}{T} \cdot \int_0^T (\Upsilon_{bypass} \cdot E_{RR}(i_{Arm,pos}))dt, \tag{A8}$$

$$P_{SW,LS} = \frac{1}{T} \cdot \int_0^T (\Upsilon_{insert} \cdot E_{On}(i_{Arm,pos}) + \Upsilon_{bypass} \cdot E_{Off}(i_{Arm,pos}))dt, \tag{A9}$$

$$P_{SW,LS,D} = \frac{1}{T} \cdot \int_0^T (\Upsilon_{insert} \cdot E_{RR}(i_{Arm,neg}))dt. \tag{A10}$$

Thermal loss model of submodule switches

$$\begin{aligned} T_{J,n} &= (R_{JC} + R_{CH} + R_{HW}) \cdot P_{T,n} + T_W, \\ P_{T,n} &= P_{C,n,} + P_{C,n,R} + P_{SW,n,} + P_{SW,n,D}. \end{aligned} \tag{A11}$$

Conduction measurement data and fit equations of model

$$\begin{aligned} V_{DS,SD} &= a_n \cdot I_D^3 + b_n \cdot I_D^2 + c_n \cdot I_D, \\ E_{On,Off,RR} &= a_m \cdot I_D^2 + b_m \cdot I_D + c_m. \end{aligned} \tag{A12}$$

Static output characteristics of 3.3 kV SiC MOSFET; definition and test circuit for dead time

Figure A1 shows the measurement output and reverse characteristics of the 3.3 kV SiC MOSFET module and the mathematical fit.

In Figure A2 the forward and reverse conduction losses are shown over the current.

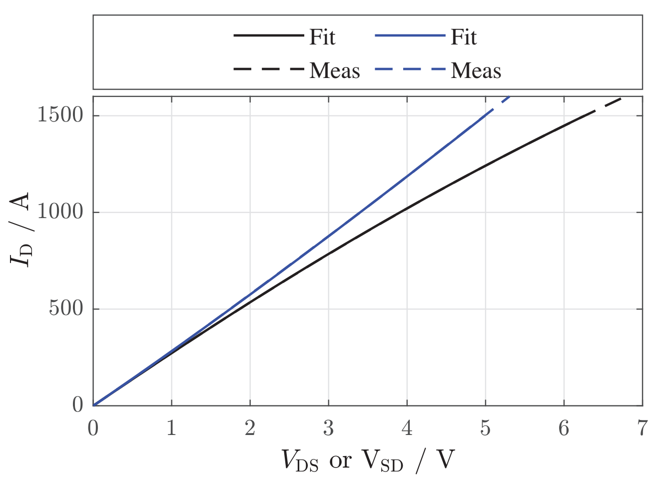

FIGURE A1 Meas. vs. Fit of 3.3 kV SiC MOSFET output (black) and reverse (blue) characteristics for $T_J = 125\,°C$, $V_{GS} = 17$ V.

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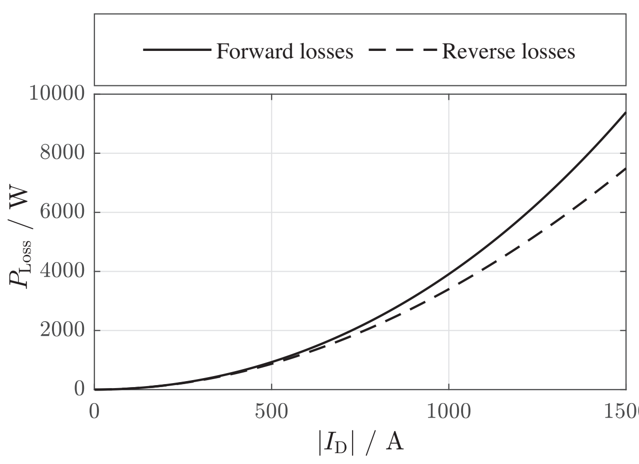

FIGURE A2 Forward and reverse conduction losses of 3.3 kV SiC MOSFET power module based on measurements in Figure A1.

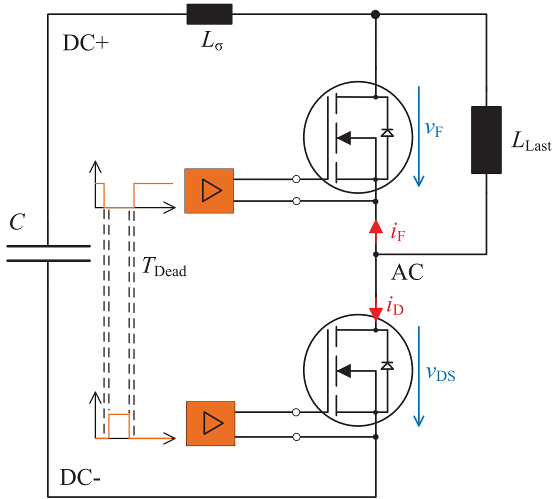

FIGURE A3 Basic test circuit for determination of the optimum dead time.

Figures A3–A5 illustrate the basic circuit for dead time tests, the basic timing diagram of the switching pulses and the detail

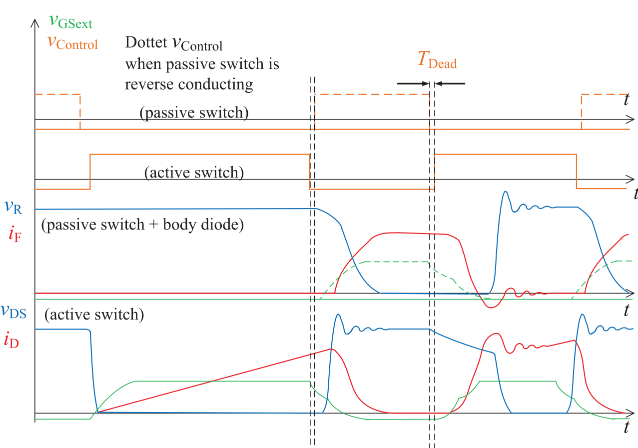

FIGURE A4 Basic overview of time diagram regarding the test setup.

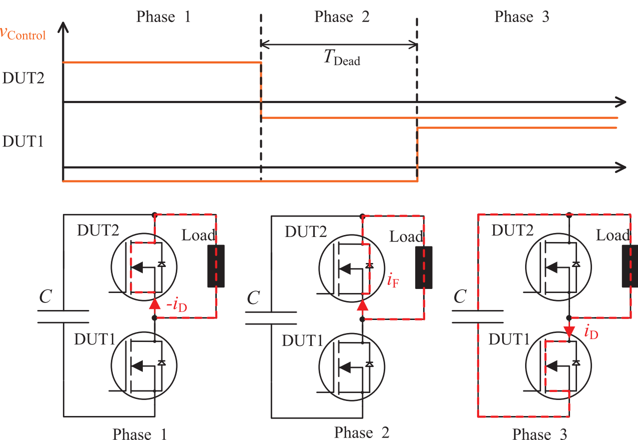

FIGURE A5 Definition and time phases of dead time.

timing definition of the dead time for reverse conduction of MOSFET channel and body diode.

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