IEEE Open Journal of
Power Electronics

Received 14 March 2023; accepted 5 April 2023. Date of publication 10 April 2023;
date of current version 21 April 2023. The review of this paper was arranged by Associate Editor Cong Li.

Digital Object Identifier 10.1109/OJPEL.2023.3265850

Junction Temperature Measurement Based on the Internal Gate Resistance for a Wide Range of Power Semiconductors

MICHAEL GLEISSNER (Senior Member, IEEE), DOMINIK NEHMER, AND MARK-M. BAKRAN (Senior Member, IEEE)

Department of Mechatronics, Center of Energy Technology, University of Bayreuth, 95447 Bayreuth, Germany

CORRESPONDING AUTHOR: MICHAEL GLEISSNER (e-mail: michael.gleissner@uni-bayreuth.de)

This article is a modification and extension of the paper presented at the PCIM Europe conference in Nuremberg 2022.

This work was supported in part by Deutsche Forschungsgemeinschaft (DFG, German Research Foundation) under Grant 491183248, and in part by the Open Access Publishing Fund of the University of Bayreuth [DOI:10.30420/565822060].

ABSTRACT This paper presents research results on the junction temperature measurement via the internal gate resistance in converter operation for IGBTs and its applicability to other types of active power semiconductors. A junction temperature monitor has been developed to determine the value of the temperature-dependent internal gate resistance by using a sinusoidal voltage superimposed on the gate voltage at the resonance frequency. The device enables a simple and robust junction temperature measurement in inverter operation, which is in excellent agreement with an infrared reference measurement. The method's applicability to semiconductors other than Si-IGBTs, such as SiC-MOSFETs, JFETs, and GaN devices, is verified by gate impedance measurements using a network analyzer. The gate impedance's quality factor is decisive. Other temperature-sensitive electrical parameters (TSEPs) related to the switching behavior depend on the internal gate resistance. Therefore, the findings presented are relevant for many junction temperature measurement methods.

INDEX TERMS Junction temperature, semiconductor device measurements, silicon carbide devices, temperature measurement, temperature-sensitive electrical parameters, wide-band-gap devices.

I. INTRODUCTION

Measuring the junction temperature of power semiconductors in practical operation can be relevant for several reasons. First, temperature measurement can detect faulty system conditions and stop operation when the maximum junction temperature is exceeded to avoid catastrophic failure. In addition, the temperature measurement during the converter operation can help to decide whether the system design is over- or even under-rated in terms of the performance of the semiconductors. The design of power electronic circuits is typically based on laboratory loss and temperature measurements and calculations based on specific load profiles [2]. The temperature measurement under real operating conditions can verify the complete design processes. In addition, temperature measurement is suggested to monitor the system's health or to detect degradation [3], [4], [5].

Power semiconductor modules often use negative or positive temperature coefficient sensors, usually soldered near the chips on the DBC ceramic substrate. The sensor value represents the base plate temperature for modules with a base plate. Sensors in modules without a base plate measure the approximate heat sink temperature. These sensors cannot capture the junction temperature because they are located too far away.

In literature, many concepts for junction temperature measurement have been proposed, either directly via housing modification or indirectly, based on temperature-sensitive electric parameters (TSEPs), which require no modification of the semiconductor package (see Fig. 1). An overview of TSEPs' sensitivity and applicability is given in [6], [7], [8]. Most of the TSEPs known for Si semiconductors have also been applied to SiC devices [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. Transfer possibilities for GaN are currently being researched [17], [20], [21], [22], [23]. Wide-band-gap devices also offer new TSEPs, like, e.g., the

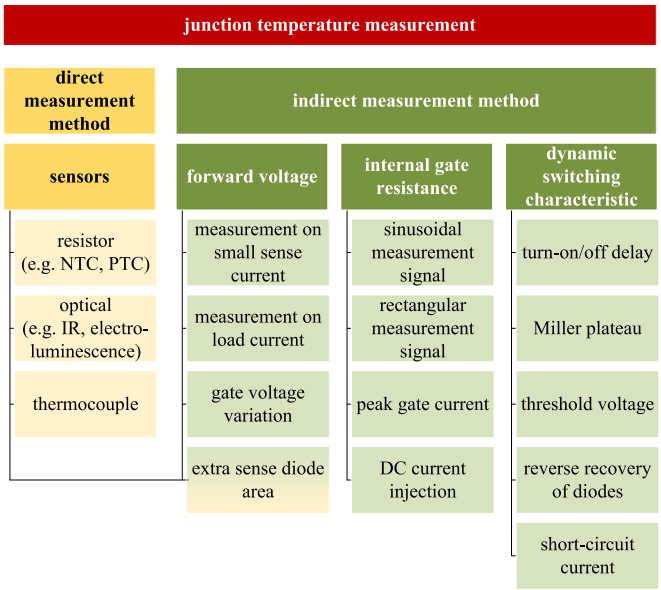

FIGURE 1. Overview of junction temperature measurement principles.

electroluminescence effect during the forward conduction interval of the SiC body diode [24], [25].

The most promising TSEP methods are either based on the forward voltage, the internal gate resistance, or changes in the dynamic switching behavior. The forward voltage can only be measured when current is flowing through the device. It also depends on the semiconductor current, which can be either a small sense or a load current. For thermal impedance measurements and degradation tests, a small sense current at a defined level is usually injected [12], [26], [27]. In converter operation, the small sense current can only be injected in idle phases [28]. An additional, accurate current sensor is necessary for online monitoring during converter operation. The temperature can be determined with a two-dimensional matching depending on measured load current, and forward voltage [29], [30], [31]. Additionally, the gate voltage can be varied to determine the temperature from the forward voltage at an equivalent current level [29]. The forward voltage can also be measured with additional diodes on the chip area, connected to a small current source [32], [33].

The problem of the current dependency does not arise with the internal gate resistor as TSEP. To prevent oscillations between parallel connected chips, many power semiconductor chips contain an internal gate resistor, typically consisting of polysilicon and located directly on the chip. Thus, the resistance value depends on the chip temperature. The internal gate resistor method cannot be applied to passive power semiconductor devices like the anti-parallel diode in IGBT inverters. Still, with the increased use of SiC-MOSFETs without parallel diodes, the significance of this drawback will decrease. The main part of the internal gate resistance normally consists of a polysilicon resistor, which is located on the semiconductor chip and has a positive temperature coefficient. The measurement of the internal gate resistance can be based on a superimposed high-frequency measurement signal on the gate voltage in either on- or off-state [11], [13], [34], [35], via DC gate current injection [36] or via measurement of the peak gate current [37], [38].

Another group of TSEPs is based on changes in the dynamic switching characteristic, which also depends on the temperature and the value of the internal gate resistance. The turn-on respectively turn-off delay as TSEP has been investigated in [16], [17], [18], [19], [39], [40], [41]. The threshold voltage can also be applied as reported in [14], [29], [42], [43], [44]. The voltage or duration of the Miller voltage plateau have also been analyzed in [40], [45]. Other dynamic switching parameters like the reverse recovery behavior [46] or the short-circuit current [47] have also been proposed as TSEPs. Most of these TSEPs based on the dynamic switching behavior have only been tested in a double pulse laboratory setup and for a specific type of semiconductor.

The internal gate resistance and the transfer characteristic of devices of the same type can vary slightly due to tolerances. The highest measuring accuracy can be achieved through a component-specific calibration for these TSEP methods. The junction temperature measurement based on the internal gate resistance is superior to other TSEPs, due to the independence from the current and the applicability to many semiconductors. In addition, it does not require high dynamic accuracy of the measuring equipment. This article shows how well the junction temperature measurement with the T_J-R_{Gi}-monitor works in converter operation with IGBTs and what needs to be considered. In addition, it is investigated and successfully demonstrated whether this method can be transferred to other semiconductor types.

The rest of the paper is organized as follows. Section II explains the operating principle of the junction temperature monitor based on the internal gate resistance. Measurement results in inverter operation with IGBTs are presented in Section III. The applicability to other semiconductor types is investigated by gate impedance measurements with a network analyzer in Section IV. In Section V, the knowledge gained from the impedance measurement is transferred to a SiC MOSFET. The temperature is recorded with the T_J-R_{Gi}-monitor during the heating and cooling phase to demonstrate how easily the thermal impedance can be determined. Finally, Section VI concludes this article.

II. OPERATING PRINCIPLE OF THE JUNCTION TEMPERATURE MONITOR

Measuring the internal gate resistance R_{Gi} enables the determination of the junction temperature of power semiconductors. The measured temperature usually correlates to the temperature of the dedicated polysilicon R_{Gi} near the gate pad. The temperature dependence of R_{Gi} is almost linear for most DUTs and has a temperature coefficient of about $\alpha_{rgi} \approx 1.0 \times 10^{-3}\,1\,K^{-1}$.

$$R_{Gi}(T_j) = R_{gi0}[1 + \alpha_{rgi} \cdot (T_j - T_0)] \quad (1)$$

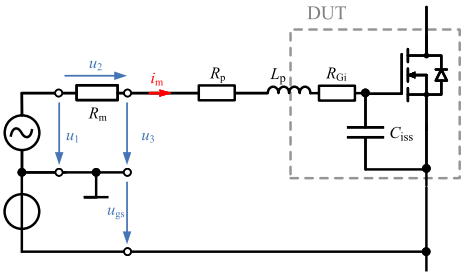

FIGURE 2. Measurement principle.

The principle of the measurement method has been first described in [48]. A driver-integrated solution has been demonstrated in [34] and a plug-and-measure device in [11]. It is outlined in Fig. 2.

By excitation with a sinusoidal voltage source, knowing u_1 and u_2, the absolute value of the gate impedance Z can be measured at an adjustable DC-gate voltage u_{gs}. If the frequency of the signal source u_1 corresponds to the resonant frequency f_{res} of the gate circuit (typically 1 to 40 MHz), the internal gate resistance R_{Gi} and the parasitic resistances R_p in the gate circuit are measured, since the imaginary parts of the parasitic stray inductance of the gate circuit L_p and the input capacitance C_{iss} cancel each other. It is:

$$\underline{u}_1 = \underline{i}_m \left(R_m + R_p + R_{Gi}(T_j) + j\omega L_p + \frac{1}{j\omega C_{iss}} \right) \quad (2)$$

$$\underline{i}_m = \underline{u}_2 / R_m \quad (3)$$

At resonance frequency $\omega_{res} = 1/\sqrt{L_p C_{iss}}$ it is:

$$R_{Gi}(T_j) + R_p = R_m \left(\frac{u_1}{u_2} - 1 \right) \quad (4)$$

The internal gate resistance on the chip has to be the dominant part of the resistance, and the parasitic resistance of, e.g., bond wires from the package pins to the die, has to be small for an excellent junction temperature measurement ($R_p << R_{Gi}(T_j)$) [49]. This is typically the case for most internal gate resistors with a value greater than 1 Ω. Further details are given in Section IV. The absolute value and the real part of an exemplary IGBT gate impedance measured with a vector network analyzer Bode 100 from OMICRON Lab, depending on the frequency and temperature, are shown in Fig. 3(a). The real part increases with frequency due to the skin effect. By adopting the sinusoidal oscillation frequency to the resonance frequency f_{res}, the ratio of measured stimulation voltage and the resulting current is equal to the real part, mainly formed by the internal gate resistance.

Based on this principle, the T_J-R_{Gi}-monitor has been designed as a measurement device, which can be installed between the gate driver and the DUT (see Fig. 4) [11]. During the measurement phase, the gate voltage is superimposed with a sinusoidal small voltage source u_1 with an amplitude of 600 mV. The current is determined via an additional measurement resistor R_m and the voltage u_3. After RMS and ADC processing, the internal gate resistance and thus temperature

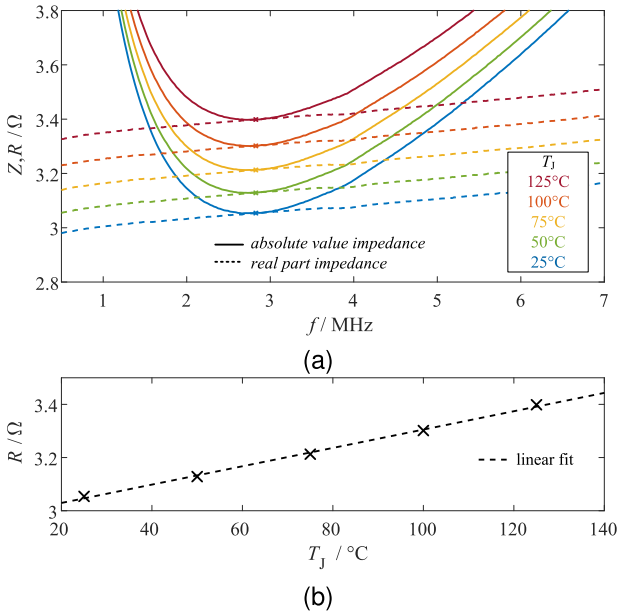

FIGURE 3. Measurement of FS200R12PT4 at $U_{GE} = -9$ V, $U_{CE} = 100$ V. The temperature is varied on a heating plate for calibration. (a) Gate impedance measurement with network analyzer Bode 100 from OMICRON Lab at varying temperature. (b) Linear dependency of resistance and temperature.

are calculated by a microcontroller STM32F303RET6 and transmitted to a PC via a fiber optic USB interface. The measurement phase is normally during the DUTs off-state in converter operation but can also be configured in on-state for thermal impedance measurements. Thus, the coupling switches S_1 and S_2 must be bidirectional. The mostly linear relationship between internal resistance and temperature (see Fig. 3(b)) typically enables a two-point calibration on a heating plate. For several semiconductors of the same type, it has been shown that the temperature coefficient is very similar. However, the absolute value of the internal gate resistance can vary slightly. For industrial use, at least a one-point calibration must be carried out, e.g., when starting the device.

The power loss within the internal gate resistance due to the superimposed measurement voltage is in the lower milliwatt range. The conduction and switching loss in the regular operation of the chip is in the range of several watts. Thus, the self-heating due to the superimposed measurement voltage can be neglected.

The measured temperature is equal to the temperature at the location of the internal gate resistance, which is typically in the center of the chip. In contrast, the temperature based on the forward voltage measurement equals the mean temperature over the total active chip area [50]. For the regular operation of chips without degradation [51], both temperatures are relatively close, as shown in the infrared measurement in Fig. 5. The infrared image of a power semiconductor with a non-uniform chip surface temperature also makes it clear that there is no single accurate junction temperature. The virtual junction temperature is sometimes used as an equivalent value determined by the forward voltage method.

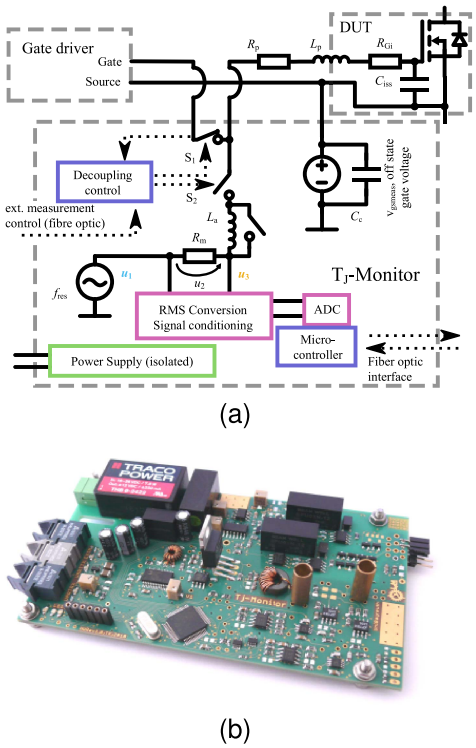

FIGURE 4. T_J-R_{Gi}-monitor: (a) Structure. (b) Circuit [11].

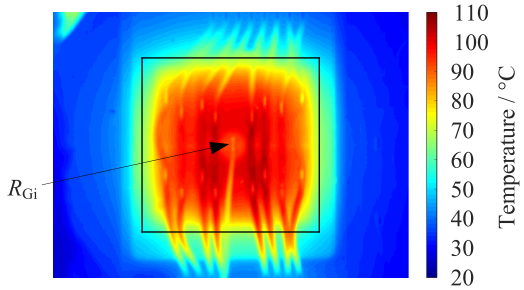

FIGURE 5. Infrared view of FS150R12KT4 chip heated with 150 A. The mean temperature of the entire chip area (black rectangle) is 87.5 °C. The temperature at the internal gate resistor in the center of the chip is 89.4 °C.

III. JUNCTION TEMPERATURE MONITOR APPLICATION WITH IGBTS

A. ONLINE JUNCTION TEMPERATURE MEASUREMENT IN CONVERTER OPERATION

The internal gate resistance is typically measured in the switch's off-state with the T_J-R_{Gi}-monitor in converter operation (see Fig. 6). Simplified, the measurement phase with duration t_{meas} starts after a delay time t_{delay} after the transition into the switch's off-state. Normally, only a single measurement value is obtained per measurement phase during the length of the ADC window t_{ADC}, which is normally at the end of t_{meas} due to a ring buffer structure implemented in the microcontroller. The ADC sample rate is 4 Megasamples per second. Optionally, consecutive ADC windows can be set to filter common mode disturbances due to other switching semiconductors within an inverter [1]. All three times t_{meas}, t_{delay} and t_{ADC} can be adjusted with the T_J-R_{Gi}-monitor. The measurement phase also includes a coupling and decoupling time, which is necessary to insert the measurement circuit between the gate driver and the DUT gate circuit (see Fig. 4(a)). If the measurement phase is longer than the switch's off time, then the T_J-R_{Gi}-monitor is immediately decoupled within 200 ns, and the measurement value is discarded. The sampling rate of the temperature measurement depends on the switching frequency, as the measurement is only once per switching period. Further limits are the transmission rate to the PC and the capability of the microcontroller, but sufficient temperature sampling rates in the range of 1 kHz to 10 kHz are feasible.

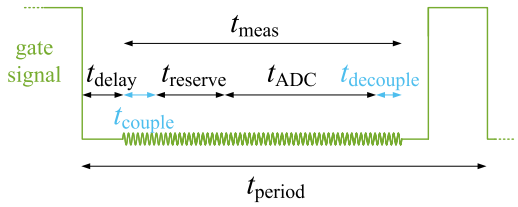

FIGURE 6. Gate signal and timing of measurement in DUT's off-state. The ADC window can be divides in several sequences to filter common mode disturbances.

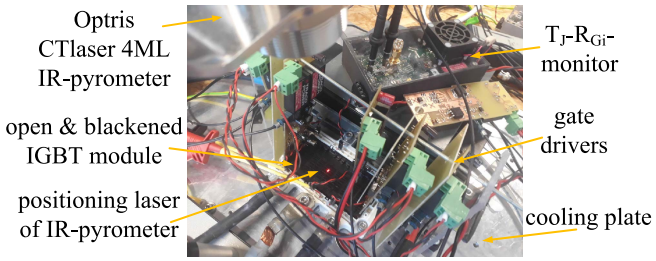

FIGURE 7. Measurement setup with open and blackened IGBT module and Optris IR-pyrometer for temperature reference.

All presented temperature measurements have been obtained with a six-pack IGBT module FS200R12PT4 in single- or three-phase inverter operation with inductive load (3x 1 mH inductors) depicted in Fig. 7. The switching frequency is 2.5 kHz. The DC-link voltage is adjusted to match the allowable current rating depending on the impedance, which varies with the output frequency.

Temperature measurements at a small output frequency of $f_{out} = 1$ Hz are helpful for a characterization of the thermal impedance because they show a relatively large ripple. The load current and temperature measurements in single-phase inverter operation are presented in Fig. 8.

Three-phase inverter temperature measurements at output frequency $f_{out} = 50$ Hz and varying modulation index are depicted in Fig. 9 at various time levels. Next to the T_J-R_{Gi}-monitor temperature value, the IR-pyrometer temperature is shown. For the IR-pyrometer measurement, the IGBT module is open and blackened (see Fig. 7) to demonstrate the perfect matching with the T_J-R_{Gi}-monitor temperature values.

The IR temperature values have a sample rate of 10 kHz. The average sampling rate of the T_J-R_{Gi}-monitor values is

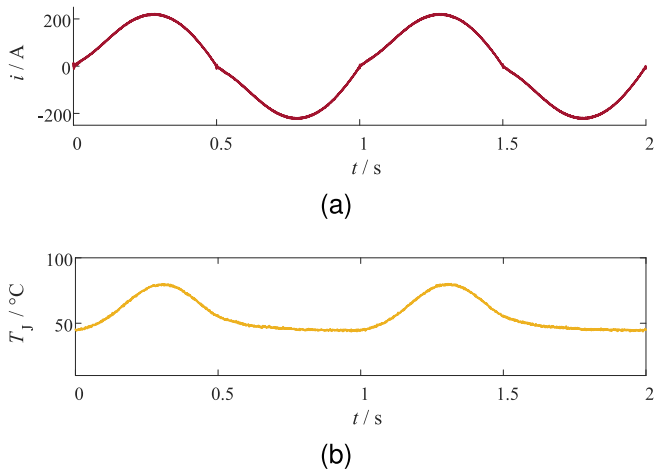

FIGURE 8. Single-phase inverter operation at $f_{out} = 1$ Hz: (a) load current. (b) Temperature measurement.

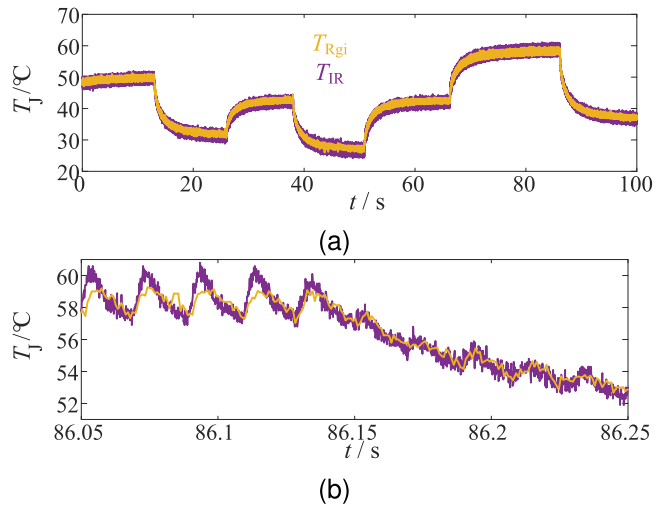

FIGURE 9. Three-phase inverter $f_{out} = 50$ Hz operation with variation of modulation index: T_J-R_{Gi}-monitor temperature measurement and IR-pyrometer reference. (a) Total view 100 s with variation of modulation index up to 60 %. (b) Zoom 200 ms.

lower due to the inverter switching frequency of 2.5 kHz limiting the measurement phase rate. The measurement shows that the T_J-R_{Gi}-monitor enables a simple and robust temperature measurement during converter operation with varying load profiles. This is confirmed by an almost perfect match with the IR-pyrometer reference measurement of a specially prepared module. The associated measurement at $f_{out} = 50$ Hz of the three-phase currents and a single output voltage of three-phase inverter operation is presented in Fig. 10.

B. SELECTING A DISTURBANCE-FREE GATE VOLTAGE

The internal gate resistance is part of the gate impedance, which is depending on the frequency due to the gate capacitance and parasitic stray inductance (see Fig. 4(a)). The gate capacitance is voltage dependent. All gate capacitances in this subsection have been measured with a Keysight Technologies

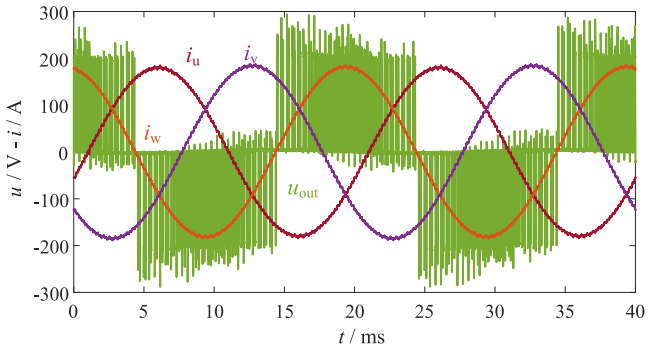

FIGURE 10. Measured phase currents and output voltage of three-phase inverter at 50 Hz operation, modulation index 50 %, $U_{DC} = 200$ V and three star connected 1 mH load inductors.

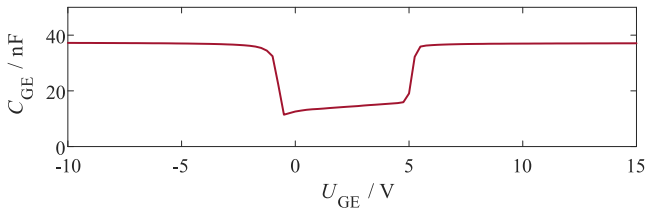

FIGURE 11. Measured IGBT gate emitter capacitance depending on gate voltage at zero blocking voltage.

power device analyzer B1506A. The flat-band effect, which shows a decreased gate capacitance in the gate voltage range of zero to five volts measured at zero blocking voltage, is well known (see Fig. 11).

But there can also be a dependency on the blocking voltage for some ranges of the gate voltage (see curve tracer measurements in Fig. 12(a) to (c)). For a gate voltage U_{GE} of 0 V or −10 V, the gate-emitter capacitance, which forms the main part of the input capacitance, is different but independent of the blocking voltage U_{CE}. For gate voltages between these boundaries, the capacitance has a blocking voltage-dependent shift. The absolute shift voltage varies with the voltage class of the here shown examples of 0.7 kV, 1.2 kV and 1.7 kV IGBT modules. The relation between shift voltage and nominal blocking voltage seems similar for all examples. Especially the often chosen gate voltage of −5 V shows the capacitance shift in typical blocking voltage ranges.

The varying capacitance leads to a shift of the resonance frequency of the gate impedance recorded with a network analyzer (see Fig. 13). Thus, the measured value of the internal gate resistance can not only depend on the chip temperature but also undesirably on parameters like the blocking voltage, which can fluctuate in real converter operation.

The effect of a wrong and good calibrated temperature measurement with the T_J-R_{Gi}-monitor in single-phase inverter operation at 50 Hz output frequency is shown in Fig. 14. With only −5 V gate voltage, the gate capacitance depends on the blocking voltage, and a 100 Hz temperature ripple due to the DC-link voltage ripple appears on the

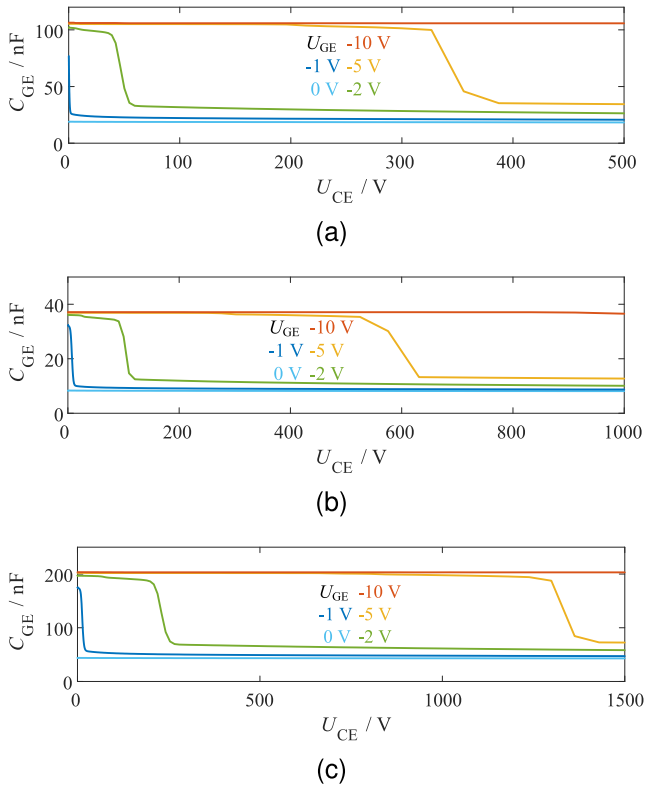

FIGURE 12. Measured IGBT gate emitter capacitance depending on gate and blocking voltage. (a) 0.7 kV IGBT module FF300R07ME4. (b) 1.2 kV IGBT module FS150R12KT4. (c) 1.7 kV IGBT module FF600R17ME4.

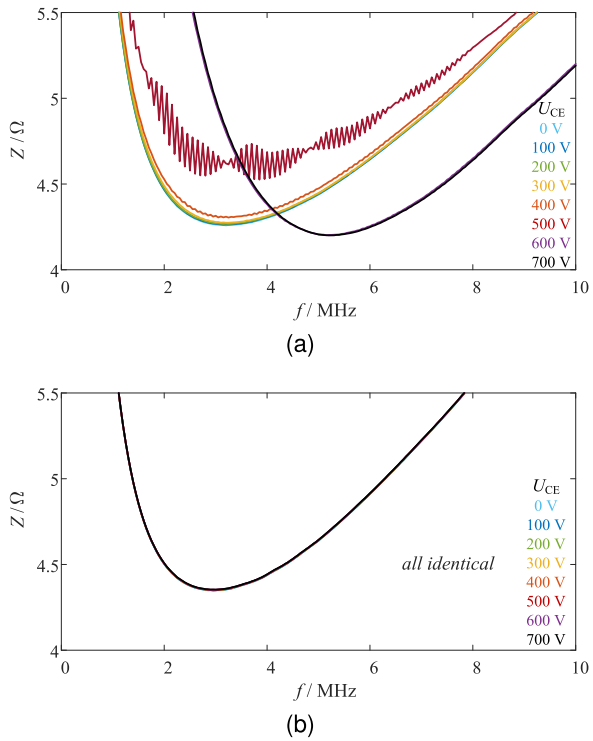

FIGURE 13. Absolute value of gate impedance of FS150R12KT4 measured with network analyzer Bode 100 from OMICRON Lab depending on gate and blocking voltage. (a) Blocking voltage dependency at $U_{GE} = -5$ V. (b) No blocking voltage dependency at $U_{GE} = -10$ V.

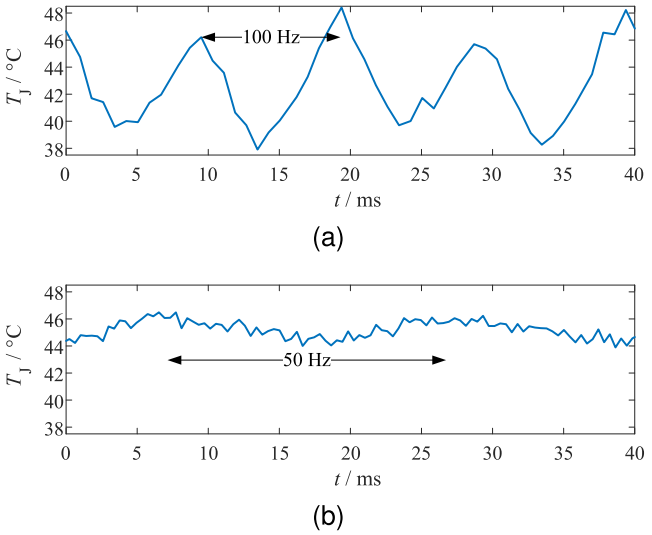

FIGURE 14. Temperature measurement with the T_J-R_{Gi}-monitor at different gate voltages in single-phase inverter operation. (a) $U_{GE} = -5$ V: additional DC-link voltage dependency. (b) $U_{GE} = -9$ V: only thermal impedance dependency.

temperature measurement. With −9 V gate voltage, only the 50 Hz ripple due to the natural thermal ripple is measured.

The optimum strategy to avoid undesired dependencies is to analyze the gate impedance with several system parameters and to choose a negative gate voltage and frequency of the superimposed measurement signal to match a point of the gate impedance, which is only temperature dependent.

IV. TESTING THE APPLICABILITY TO OTHER SEMICONDUCTORS BY GATE IMPEDANCE MEASUREMENT

The applicability of the R_{Gi}-method to other semiconductors than IGBTs like SiC-MOSFETs or GaN devices is analyzed in this section by gate impedance measurements with a vector network analyzer Bode 100 from OMICRON Lab. The network analyzer can determine the absolute value and the real part of the gate impedance. However, the accuracy of the real part far from the resonant point drops significantly. In a simple LCR series resonant circuit, the real part corresponds to the ohmic part of the impedance.

A. SILICONE CARBIDE MOSFETS

In [11] a characteristic of the gate impedance of SiC-MOSFETs was described, which cannot be justified with a simple series connection of *LCR*. A decrease of the real part at lower frequencies and a change in the sign of the temperature coefficient have been reported. Reasons for this can be gate interference traps or the base material of the gate resistor with other properties. This characteristic of the real part can be modeled by adding a parallel *RC* element in series with the *LCR* element (see Fig. 15) [49].

The gate impedance of several 1.2 kVSiC-MOSFETs from different manufacturers has been analyzed. Relevant parameters of the semiconductors are listed in Table 1. Fig. 16

TABLE 1. Parameters of Investigated 1.2 kV SiC MOSFETs

manufacturer	type	$R_{DS,on}$ / Ω	I_N / A	TO package	f_{res} / MHz	R_{res} / Ω	C_{iss} / pF	L / nH	Q
STMicroelectronics	SCTW70N120G2V	21	91	247-3	23.1	0.95	3230	15	2.3
Rohm	SCT3022KL	22	95	247-3	21.2	1.71	3306	17	1.3
Wolfspeed	C3M0016120D	16	112	247-3	17.7	1.81	7282	11	0.7
Wolfspeed	C3M0016120K	16	112	247-4	26.7	1.62	7489	5	0.5
Wolfspeed	C2M0080120D	80	36	247-3	33.5	2.81	1194	19	1.4
Infineon	IMZA120R014M1H	14	127	247-4	19.5	3.56	5095	13	0.5
Infineon	IMW120R045M1	45	52	247-3	24.0	2.56	2086	21	1.2

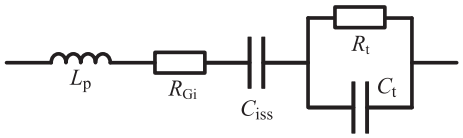

FIGURE 15. Extended equivalent circuit for SiC MOSFET gate impedance to model trapping effects [49].

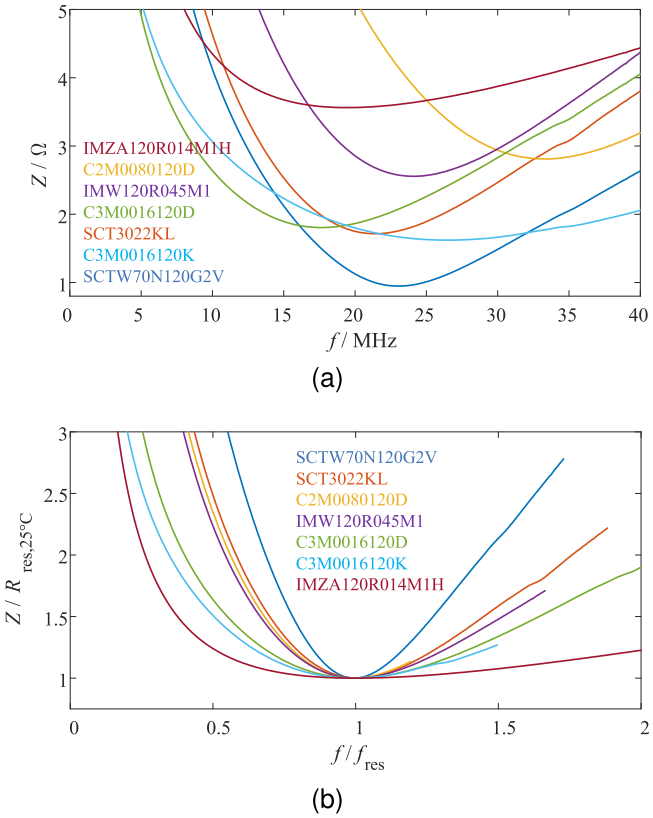

FIGURE 16. Absolute value of gate impedance measured with network analyzer Bode 100 from OMICRON Lab of 1.2 kV SiC-MOSFET in TO-247 package at −5 V gate and 100 V blocking voltage for various manufacturers and generation versions at 25 °C: a) absolute values, b) normalized absolute values.

gives an overview of the general characteristic of the 1.2 kV SiC-MOSFET gate impedance curves at room temperature. The impedance at resonance is in the range of 1 Ω to 4 Ω and the resonance frequency varies between 17 MHz to 34 MHz. The temperature dependency of the impedance at resonance frequency is illustrated in Fig. 17.

Detailed views of the measured gate impedance including absolute value and and real part at various temperatures are

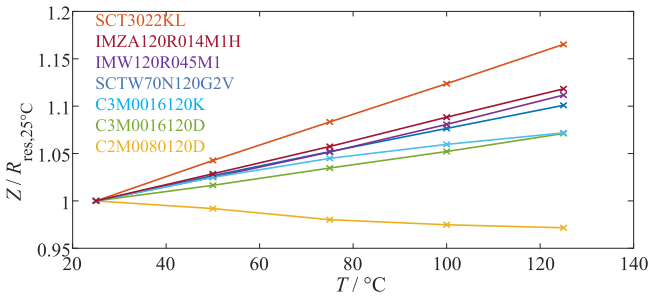

FIGURE 17. Measured temperature dependency of the gate impedance at resonance frequency of 1.2 kV SiC-MOSFETs.

shown in Fig. 18. The present state-of-the-art types of all four investigated manufacturers (see Fig. 18(a) to (e)) show that there is a mostly linear temperature dependency in the range of the resonance frequency, which can be utilized for temperature measurement with the T_J-R_{Gi}-monitor. The package layout with an additional Kelvin source pin has no significant influence on the shape of the measured curves except a higher resonance frequency due to the smaller gate inductance (see Fig. 18(c) versus Fig. 18(e)). The older chip generation of Infineon shows a more pronounced effect of the isothermal point with a shift of the sign of the temperature coefficient (see Fig. 18(d) versus Fig. 18(f)). The outdated generation in Fig. 18(g) shows, in contrast to all other samples, a negative temperature coefficient over the total frequency range. The frequency f_{res} and the resistance R_{res} at resonance have been measured with a network analyzer. The input capacitance C_{iss} has been determined with a curve tracer at −5 V gate and 100 V blocking voltage. The gate circuit inductance L and the quality factor Q have been calculated from these three values based on a serial LCR network and constant parameters.

With SiC-MOSFETs, as with all other semiconductors, an analysis of the gate impedance must be carried out to ensure that there is only a temperature dependency by selecting a suitable gate voltage.

B. JFETS

The unique feature of the gate circuit of the JFET compared to IGBT and MOSFET is the nonexistent oxide and, instead, the blocking diode with its capacitance. The measured gate impedance of a 1.2 kV SiC JFET is depicted in Fig. 19. Further details on the normally-on SiC JFET are given in Table 2. The temperature sensitivity of the gate impedance (see also Fig. 24) enables temperature measurement with the T_J-R_{Gi}-monitor.

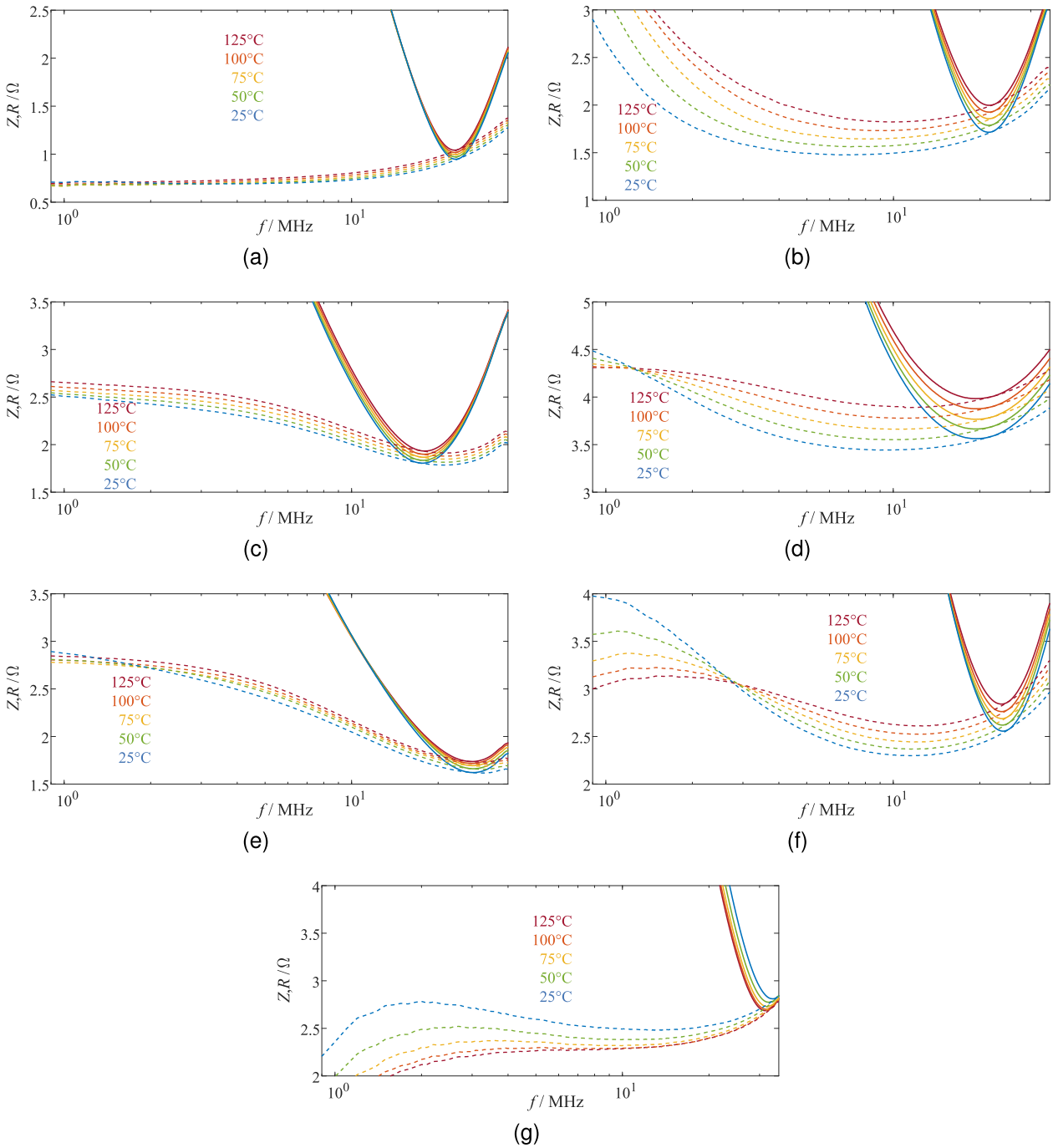

FIGURE 18. Gate impedance measured with network analyzer Bode 100 from OMICRON Lab: absolute value (full line) and real part (dashed line) of 1.2 kV SiC-MOSFETs in TO-247 package at −5 V gate and 100 V blocking voltage for various manufacturers and generation versions at different temperatures. (a) STMicroelectronics SCTW70N120G2V, (b) Rohm SCT3022KL, (c) Wolfspeed C3M0016120D, (d) Infineon IMZA120R014M1H, (e) Wolfspeed C3M0016120 K, (f) Infineon IMW120R045M1, (g) Wolfspeed C2M0080120D.

TABLE 2. Parameters of Investigated Semiconductors With Varying Technology. The * Values are Obtained by Subtraction of an Additional Inductance With 190 nH and 350 mΩ

manufacturer	type	semiconductor	I_N / A	U_{max} / V	package	f_{res} / MHz	R_{res} / Ω	C_{iss} / pF	L / nH	Q
Infineon	IKW50N60DTP	IGBT	50	600	TO 247-3	9.7	0.82	12562	22	1.6
Infineon	FS200R12PT4	IGBT	200	1200	module	2.8	3.05	49763	69	0.4
Infineon	IGOT60R070D1	eGaN	31	600	PG-DSO-20-87	84*	0.90	360	10*	5.9
Infineon	IGOT60R070D1	eGaN	31	600	PG-DSO-20-87	18.9	1.25	360	200	18.7
Nexperia	GAN041-650WSB	GaN cascode	47.2	650	TO 247-3	32.5	1.74	1782	13	1.6
UnitedSiC	UJ4N120008K3S	SiC JFET	120	1200	TO 247-3	21.8	0.84	3621	15	2.4
UnitedSiC	UF3SC120009K4S	JFET cascode	120	1200	TO 247-4	16.7	1.01	9325	10	1.0

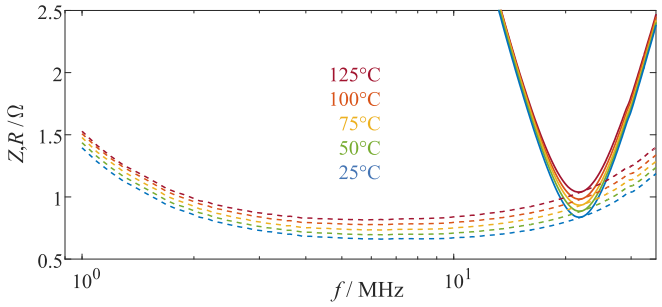

FIGURE 19. Gate impedance measured with network analyzer Bode 100 from OMICRON Lab: absolute value (full line) and real part (dashed line) of UnitedSiC UJ4N120008K3S normally-on SiC JFETs at −18 V gate and 100 V blocking voltage at different temperatures.

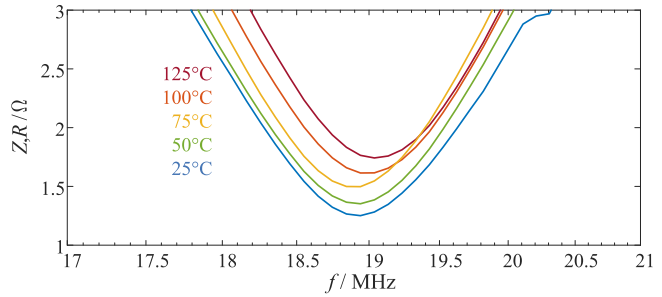

FIGURE 20. Absolute value of gate impedance measured with network analyzer Bode 100 from OMICRON Lab of Infineon IGOT60R070D1 enhancement mode GaN at −5 V gate and 100 V blocking voltage at different temperatures with additional inductance 190 nH and 350 mΩ at 18.9 MHz.

C. GAN

GaN devices are designed to have a very low inductance gate and commutation loop [52] in the range of less than 10 nH. In conjunction with a minimal input capacitance, this leads to very high resonance frequencies, which make a measurement with the T_J-R_{Gi}-monitor difficult. Fig. 20 illustrates the measured gate impedance of a 600 V enhancement GaN from Infineon (see Table 2) with an additional inductance of 190 nH and 350 mΩ at 18.9 MHz. Without this additional gate inductance, the resonance frequency is far beyond the maximum frequency of the OMICRON Lab Bode 100 network analyzer. The gate impedance shows a temperature dependency, but with the additional inductance, the quality factor of the LCR network increases and results in a very sharp impedance curve according to:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{5}$$

D. CASCODE STRUCTURE DEVICES

Cascode structures are applied to convert normally-on devices like JFETs or depletion mode GaN HEMTs to normally-off devices. Therefore, a Si MOSFET is connected in series (see Fig. 21). This MOSFET determines the gate impedance characteristic. The temperature dependency of a GaN HEMT cascode is shown in Fig. 22(a) and of a SiC JFET cascode in Fig. 22(b). Both characteristics enable a temperature measurement via the internal gate resistance.

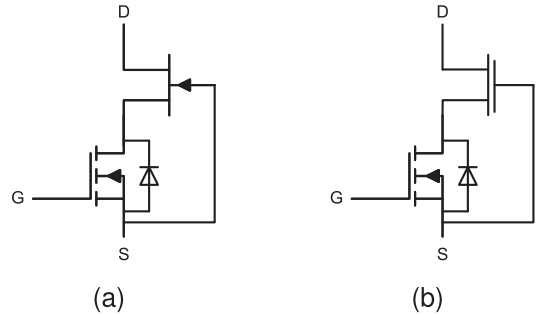

FIGURE 21. Cascode structure with Si MOSFET (bottom) and a) normally-on JFET, b) depletion mode GaN HEMT.

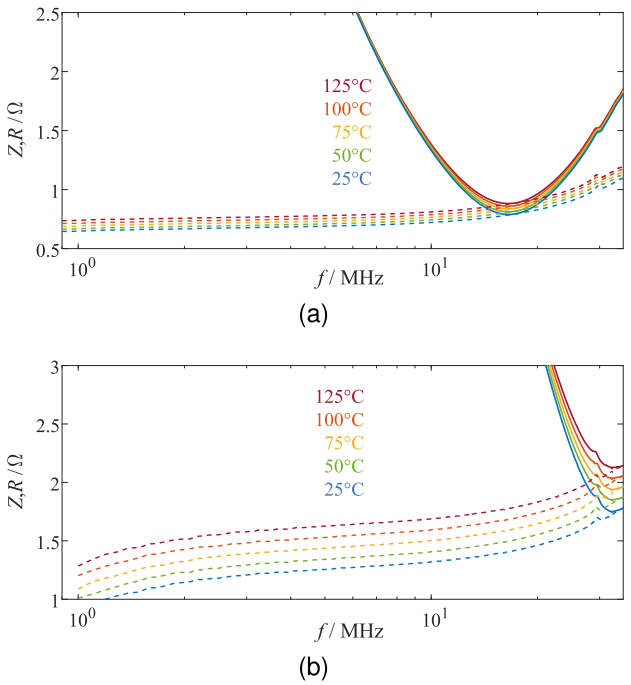

FIGURE 22. Gate impedance measured with network analyzer Bode 100 from OMICRON Lab: absolute value (full line) and real part (dashed line) of cascaded semiconductors at −5 V gate and 100 V blocking voltage at different temperatures. (a) UnitedSiC UF3SC120009K4S SiC JFET cascode, (b) Nexperia GAN041-650WSB GaN HEMT cascode.

E. OVERVIEW

The general characteristic of several gate impedance curves at room temperature of selected devices GaN, SiC JFET, and cascode devices from Tables 1 and 2 is illustrated in Fig. 23. The impedance curve becomes flatter with decreasing quality factor. A flatter impedance curve makes it easier to measure the temperature with the T_J-R_{Gi}-monitor since the resonance point does not have to be hit precisely. By inserting an additional inductance in the measurement circuit, the resonance frequency can be decreased, but as a disadvantage, the quality factor and the temperature sensitivity decrease due to the parasitic resistance of the inductance. The temperature sensitivity

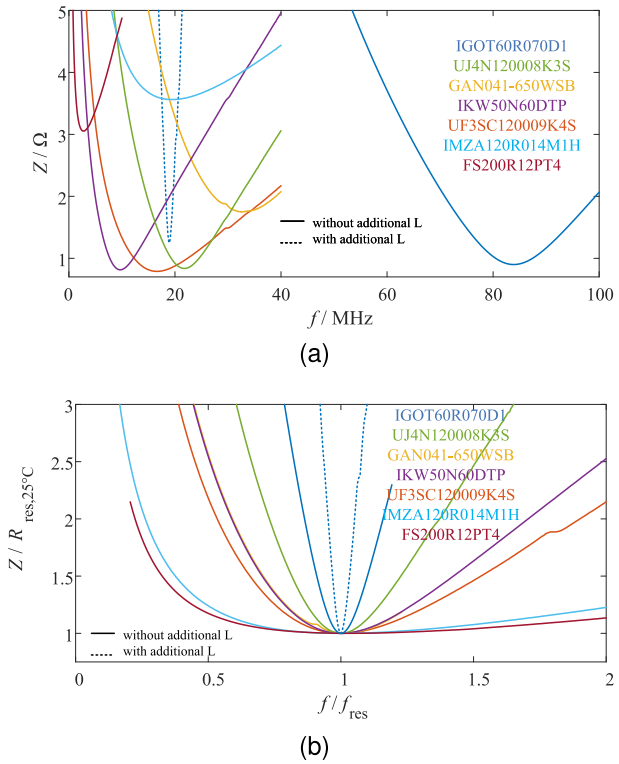

FIGURE 23. Absolute value of gate impedance measured with network analyzer Bode 100 from OMICRON Lab of various semiconductor types at 25 °C: (a) absolute values, (b) normalized absolute values.

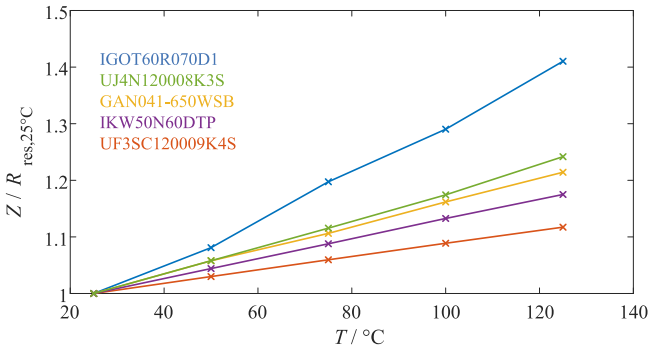

FIGURE 24. Measured temperature dependency of the gate impedance at resonance frequency of various semiconductor types.

of the measured devices at resonance frequency is illustrated in Fig. 24.

V. JUNCTION TEMPERATURE MONITOR APPLICATION WITH SIC MOSFET

Based on the findings of the gate impedance measurements from the previous section, the applicability of the T_J-R_{Gi}-monitor to wide-bandgap semiconductors is now shown using a SiC MOSFET as an example. In contrast to inverter operation, as in Section III, another application example shows how easily the thermal impedance can be determined with the T_J-R_{Gi}-monitor by recording cooling or heating curves.

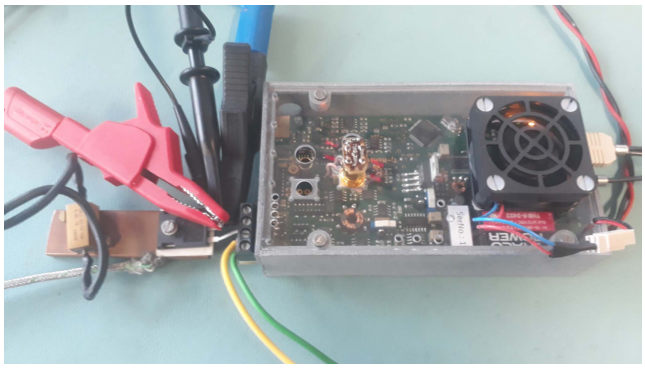

FIGURE 25. Thermal impedance measurement setup of TO SiC MOSFET with T_J-R_{Gi}-monitor. The DUT in a TO package is mounted on a heating plate for the calibration. For measurement phases, the heating plate can be removed.

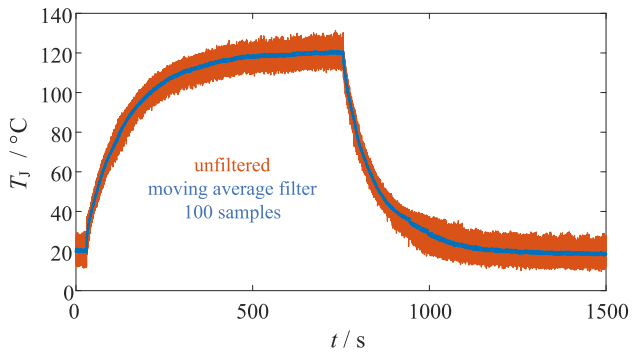

FIGURE 26. Measured junction temperature with T_J-R_{Gi}-monitor during heating phase with 13 A drain current and cooldown of SiC-MOSFET C3M0016120D.

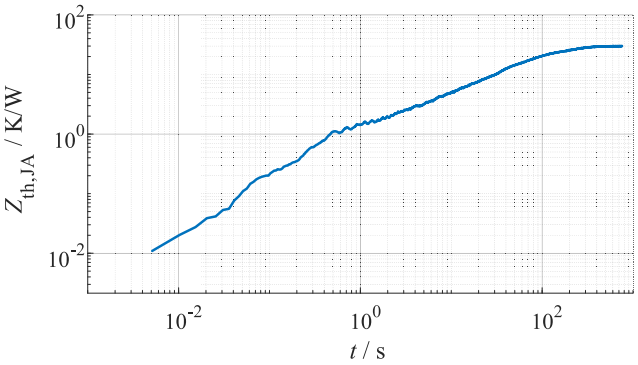

FIGURE 27. Thermal impedance measurement based on cooldown phase of junction temperature measurement based on R_{Gi}-method.

The junction temperature is usually measured by the forward voltage on a small sense current during a cooling down period after heating the device to a steady state to determine the thermal impedance of power semiconductors. For on-state SiC MOSFETs with small measurement currents, the voltage to be measured is very low due to the lack of threshold voltage and low $R_{DS,on}$ [10]. In the off state, the body diode can be used in the reverse direction. To do this, the gate voltage must be sufficiently negative for the prevention

of the influence of the channel [9]. The thermal impedance $Z_{th}(t)$ can be calculated from the cooling temperature curve $T(t)$, the initial temperature in stationary mode T_{init} and the heating power P, which the product of collector current and forward voltage can determine:

$$Z_{th}(t) = \frac{T_{init} - T(t)}{P} \tag{6}$$

To enable a fast commutation between a large heating current and a small sense current typically in the range of 1 to 100 mA, an additional serial and parallel switch are added to the test setup. Nevertheless, there can be a short blind time with the forward voltage method, e.g., due to the recombination of charge carriers in IGBTs within the first hundreds of microseconds [27], [50], [53], [54]. A linear evolution can obtain the relevant starting temperature with the square root of time [53], [55], [56], which is a good approximation for a power density up to 300 $\mathrm{Wcm^{-2}}$.

Alternatively, the junction temperature can be measured with the T_J-R_{Gi}-monitor. Here, the T_J-R_{Gi}-monitor is configured for measurement during the on-state of the DUT at a positive gate voltage (see Fig. 25). The SiC-MOSFET C3M0016120D within a TO package is here mounted on a copper heating plate for the calibration of the T_J-R_{Gi}-monitor. The linear dependency of the resistance on the temperature of the gate impedance measurements (see Fig. 17) can be confirmed with the T_J-R_{Gi}-monitor.

Fig. 26 shows the measured heating and cool-down temperature of the SiC-MOSFET within a TO package. The heating plate for the calibration has been removed, and the device is heated by a current of 13 A in permanent on mode. The sample rate of the raw data is 200 Hz and can be increased to 50 kHz for the first samples after triggering the measurement. The bottle neck is the transfer rate of the T_J-R_{Gi}-monitor to the PC. A filter like a moving average can significantly remove the large temperature ripple of the raw data. The R_{Gi}-method enables a continuous temperature measurement during the heating and cooling phases. In contrast, the forward voltage method typically only measures cooling down phases and has a blind time of 150 µs to 1 ms after load current turn-off due to the recombination time from the high heating current to the small sense current [53]. A $\sqrt{t}$-extrapolation has to be applied to determine the initial temperature for the forward voltage method. The T_J-R_{Gi}-monitor can measure the temperature at all times.

The thermal impedance junction to the ambient of the TO package without any cooling plate based on the cooldown temperature measurement is depicted in Fig. 27. The T_J-R_{Gi}-monitor enables a fast and straightforward method of thermal impedance measurement without any additional switches to speed up the recombination process between heating and sense current or extrapolation to the starting value.

VI. CONCLUSION

The junction temperature measurement via the internal gate resistance is a promising method, which requires no modification of the package and enables a fast integration in existing converter configurations with the presented T_J-R_{Gi}-monitor.

The problem of further dependencies on system variables like e.g. the blocking voltage is presented in this paper for several IGBT voltage classes. This unwanted effect can be excluded by an analysis of the gate impedance and the choice of an optimal gate voltage in the off-state, where the internal gate resistance is measured.

The investigation of the gate impedance of several semiconductor types from various manufacturers has shown, that the junction temperature monitor can be applied to a wide range of devices.

REFERENCES

[1] M. Gleissner and M.-M. Bakran, "Special effects of junction temperature measurement based on the internal gate resistance," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Inst. Renewable Energy Energy Manage.*, 2022, pp. 1–10.

[2] N. Baker, M. Liserre, L. Dupont, and Y. Avenas, "Improved reliability of power modules: A review of online junction temperature measurement methods," *IEEE Ind. Electron. Mag.*, vol. 8, no. 3, pp. 17–27, Sep. 2014.

[3] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.

[4] K. Wei, W. Wang, Z. Hu, and M. Du, "Condition monitoring of IGBT modules based on changes of thermal characteristics," *IEEE Access*, vol. 7, pp. 47525–47534, 2019.

[5] C. H. van der Broeck, T. A. Polom, R. D. Lorenz, and R. W. de Doncker, "Real-time monitoring of thermal response and life-time varying parameters in power modules," *IEEE Trans. Ind. Appl.*, vol. 56, no. 5, pp. 5279–5291, Sep.–Oct. 2020.

[6] J. Brandelero, J. Ewanchuk, and S. Mollov, "Online junction temperature measurements for power cycling power modules with high switching frequencies," in *Proc. IEEE 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 191–194.

[7] H. Niu and R. D. Lorenz, "Evaluating different implementations of online junction temperature sensing for switching power semiconductors," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 391–401, Jan./Feb. 2017.

[8] C. Chen, V. Pickert, B. Ji, C. Jia, A. C. Knoll, and C. Ng, "Comparison of TSEP performances operating at homogeneous and inhomogeneous temperature distribution in multichip IGBT power modules," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 6282–6292, Oct. 2021.

[9] T. Kestler and M. Bakran, "Junction temperature measurement of SiC MOSFETs: Straightforward as it seems?," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage. (PCIM Europe)*. 2018, pp. 1–6.

[10] F. Stella, G. Pellegrino, E. Armando, and D. Dapra, "Online junction temperature estimation of SiC power MOSFETs through on-state voltage mapping," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3453–3462, Jul./Aug. 2018.

[11] T. Kestler and M.. Bakran, "A plug and measure device for junction temperature monitoring in real converter environment," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage. (PCIM Europe)*, 2019, pp. 2025–2030.

[12] B. Shi et al., "Junction temperature measurement method for SiC bipolar junction transistor using base–collector voltage drop at low current," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10136–10142, Oct. 2019.

[13] J. Ruthardt et al., "Investigations on online junction temperature measurement for SiC-MOSFETs using the gate-signal injection method," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2021, pp. 5354–5359.

[14] X. Jiang et al., "Online junction temperature measurement for SiC MOSFET based on dynamic threshold voltage extraction," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3757–3768, Apr. 2021.

[15] J. O. Gonzalez and O. Alatise, "Bias temperature instability and junction temperature measurement using electrical parameters in SiC power MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 57, no. 2, pp. 1664–1676, Mar./Apr. 2021.

[16] Z. Zhang et al., "Online junction temperature monitoring using intelligent gate drive for SiC power devices," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7922–7932, Aug. 2019.

[17] K. Sharma, K. M. Barón, J. Ruthardt, and I. Kallfass, "Online junction temperature monitoring of wide bandgap power transistors using quasi turn-on delay as TSEP," in *Proc. IEEE 8th Workshop Wide Bandgap Power Devices Appl.*, 2021, pp. 129–134.

[18] F. Yang, S. Pu, C. Xu, and B. Akin, "Turn-on delay based real-time junction temperature measurement for SiC MOSFETs with aging compensation," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1280–1294, Feb. 2021.

[19] P. Sun et al., "An online junction temperature monitoring correction method for SiC MOSFETs at different parasitic parameters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5007–5018, Oct. 2022.

[20] A. Borghese, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate driver for p-GaN HEMTs with real-time monitoring capability of channel temperature," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 63–66.

[21] A. Borghese, A. Di Costanzo, M. Riccio, L. Maresca, G. Breglio, and A. Irace, "Gate current in p-GaN gate HEMTs as a channel temperature sensitive parameter: A. comparative study between schottky- and ohmic-gate GaN HEMTs," *Energies*, vol. 14, no. 23, 2021, Art. no. 8055.

[22] X. Li et al., "A drain–source connection technique: Thermal resistance measurement method for GaN HEMTs using TSEP at high voltage," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5454–5459, Dec. 2020.

[23] L. Zhang, P. Liu, S. Guo, and A. Q. Huang, "Comparative study of temperature sensitive electrical parameters (TSEP) of Si, SiC and GaN power devices," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, 2016, pp. 302–307.

[24] C. Li, H. Luo, C. Li, W. Li, H. Yang, and X. He, "Online junction temperature extraction of SiC power MOSFETs with temperature sensitive optic parameter (TSOP) approach," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10143–10152, Oct. 2019.

[25] H. Luo, J. Mao, C. Li, F. Iannuzzo, W. Li, and X. He, "Online junction temperature and current simultaneous extraction for SiC MOSFETs with electroluminescence effect," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 21–25, Jan. 2022.

[26] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. IEEE 2nd Int. Conf. Power Electron. Drive Syst.*, 1997, pp. 425–430.

[27] G. Zeng, H. Cao, W. Chen, and J. Lutz, "Difference in device temperature determination using p-n-junction forward voltage and gate threshold voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2781–2793, Mar. 2019.

[28] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "In situ diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.

[29] L. Dupont and Y. Avenas, "Evaluation of thermo-sensitive electrical parameters based on the forward voltage for on-line chip temperature measurements of IGBT devices," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 4028–4035.

[30] P. Ghimire, K. B. Pedersen, A. R. d. Vega, B. Rannestad, S. Munk-Nielsen, and P. B. Thogersen, "A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application," in *Proc. IEEE 8th Int. Conf. Integr. Power Electron. Syst.*, 2014, pp. 1–6.

[31] A. Bryant, "Simplifying the calibration of on-state voltage drop for online junction temperature estimation in an industrial context," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2020, pp. 1–8.

[32] C. Kempiak, A. Lindemann, S. Idaka, and E. Thal, "Investigation of an integrated sensor to determine junction temperature of SiC MOSFETs during power cycling tests," in *Proc. IEEE 10th Int. Conf. Power Electron. ECCE Asia*, 2019, pp. 3084–3089.

[33] R. Mitova, A. Bel Hadj, and A. Dentella, "Evaluation of IGBT with integrated temperature sensor for on-line junction temperature monitoring," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2020, pp. 1–7.

[34] M. Denk and M.-M. Bakran, "Junction temperature measurement during inverter operation using a Tj-IGBT-Driver," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2015, pp. 818–825.

[35] J. Ruthardt et al., "Online junction temperature measurement via internal gate resistance using the high frequency gate signal injection method," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion Renew. Energy Energy Manage.*, 2019, pp. 900–906.

[36] J. Brandelero, J. Ewanchuk, and S. Mollov, "On-line virtual junction temperature measurement via DC gate current injection," in *Proc. IEEE 10th Int. Conf. Integr. Power Electron. Syst.*, 2018, pp. 1–7.

[37] N. Baker, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IGBT junction temperature measurement via peak gate current," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3784–3793, May 2016.

[38] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IR camera validation of IGBT junction temperature measurement via peak gate current," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3099–3111, Apr. 2017.

[39] H. Kuhn and A. Mertens, "On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters," in *Proc. IEEE 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.

[40] J. A. Butron Ccoa, B. Strauss, G. Mitic, and A. Lindemann, "Investigation of temperature sensitive electrical parameters for power semiconductors (IGBT) in real-time applications," in *Proc. IEEE Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, 2014, pp. 1–9.

[41] H. Luo, Y. Chen, P. Sun, W. Li, and X. He, "Junction temperature extraction approach with turn-off delay time for high-voltage high-power IGBT modules," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5122–5132, Jul. 2016.

[42] Y. Bayarsaikhan and I. Omura, "Dynamic VGS-id monitoring system for junction temperature estimation for MOS gate power semiconductors," in *Proc. IEEE 34th Int. Symp. Power Semicond. Devices ICs*, 2022, pp. 193–196.

[43] D. Blackburn and D. W. Berning, "Power MOSFET temperature measurements," in *Proc. IEEE Power Electron. Specialists Conf.*, 1982, pp. 400–407.

[44] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power MOSFETs considering thermal aging effects," *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 1, pp. 220–228, Mar. 2014.

[45] V. Sundaramoorthy, E. Bianda, R. Bloch, I. Nistor, G. Knapp, and A. Heinemann, "Online estimation of IGBT junction temperature (TJ) using gate-emitter voltage (VGE) at turn-off," in *Proc. IEEE 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–10.

[46] J. Ruthardt, K. Sharma, T. Schmid, M. Nitzsche, P. Ziegler, and J. Roth-Stielow, "Online junction temperature measurement of power semiconductor devices," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage*, 2020, pp. 1–5.

[47] Z. Xu, F. Xu, and F. Wang, "Junction temperature measurement of IGBTs using short circuit current as a temperature sensitive electrical parameter for converter prototype evaluation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3419–3429, Jun. 2015.

[48] E. Hoene, T. Baumann, and O. Zeiter, "Device for measuring a temperature of a power semiconductor," U.S. Patent 2014/0112372 A1, Apr. 24, 2014.

[49] T. Kestler and M.-M. Bakran, "Expansion of the junction temperature measurement via the internal gate resistance to a wide range of power semiconductors," in *Proc. IEEE 21st Eur. Conf. Power Electron. Appl.*, 2019, pp. P.1–P.9.

[50] M. Denk and M.-M. Bakran, "Comparison of UCE- and RGi-based junction temperature measurement of multichip IGBT power modules," in *Proc. IEEE 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–11.

[51] M. Gleissner, O. Schilling, and M.-M. Bakran, "Perceptibility comparison of degraded thermal parameters of a power module by junction temperature measurement via the internal gate resistance and forward voltage," in *Proc. IEEE 23rd Eur. Conf. Power Electron. Appl.*, 2021, pp. 1–9. [Online]. Available: urlhttps://ieeexplore.ieee.org/document/9570619

[52] D. Reusch and J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2008–2015, Apr. 2014.
[53] C. Herold, M. Beier, J. Lutz, and A. Hensler, "Improving the accuracy of junction temperature measurement with the square-root-t method," in *Proc. IEEE 19th Int. Workshop Thermal Investigations ICs Syst.*, 2013, pp. 92–94.
[54] W. Chen, J. Franke, C. Herold, R. Bhojani, and J. Lutz, "Internal processes in power semiconductors at virtual junction temperature measurement," *Microelectronics Rel.*, vol. 64, pp. 464–468, 2016.
[55] D. L. Blackburn and F. F. Oettinger, "Transient thermal response measurements of power transistors," *IEEE Trans. Ind. Electron. Control Instrum.*, vol. IECI-22, no. 2, pp. 134–141, May 1975.
[56] E. Deng and J. Lutz, "Measurement error caused by the square root T method applied to IGBT devices during power cycling test," in *Proc. IEEE 32nd Int. Symp. Power Semicond. Devices ICs*, 2020, pp. 545–548.

MICHAEL GLEISSNER (Senior Member, IEEE) received the Diploma in electrical engineering and information technology with the University of Applied Sciences Ingolstadt, Ingolstadt, Germany, in 2010, and the Dr.-Ing. degree from the University of Bayreuth, Bayreuth, Germany, in 2016. He is currently a Senior Lecturer with the Department of Mechatronics, University of Bayreuth. His research interests include safe power electronics including fault-tolerance, failure characteristics, and temperature measurement.

DOMINIK NEHMER received the master's degree in electrical engineering, electronics, information technology with the Friedrich-Alexander-Universität Erlangen-Nürnberg, Erlangen, Germany, in 2020. He is currently a Research Associate with the Department of Mechatronics, University of Bayreuth, Bayreuth. His research focuses wide-bandgap power semiconductors in traction converters.

MARK-M. BAKRAN (Senior Member, IEEE) received the Diploma and the Dr.-Ing. degree in electrical engineering from the Technical University of Berlin, Berlin, Germany, in 1992 and 1995, respectively. From 1995 to 2011, he was with Siemens AG, Germany. Within the Traction Division, he was responsible for power electronics from auxiliary converters to hybrid buses and from light rail vehicles to locomotives. In 2011, he became an Appointed Professor with the University of Bayreuth, Bayreuth, Germany.